

# Quanta Confidential

## KBL-U/R MB Schematic Document

**ZAT**

**Rev: 5A**

**2019.03.20**



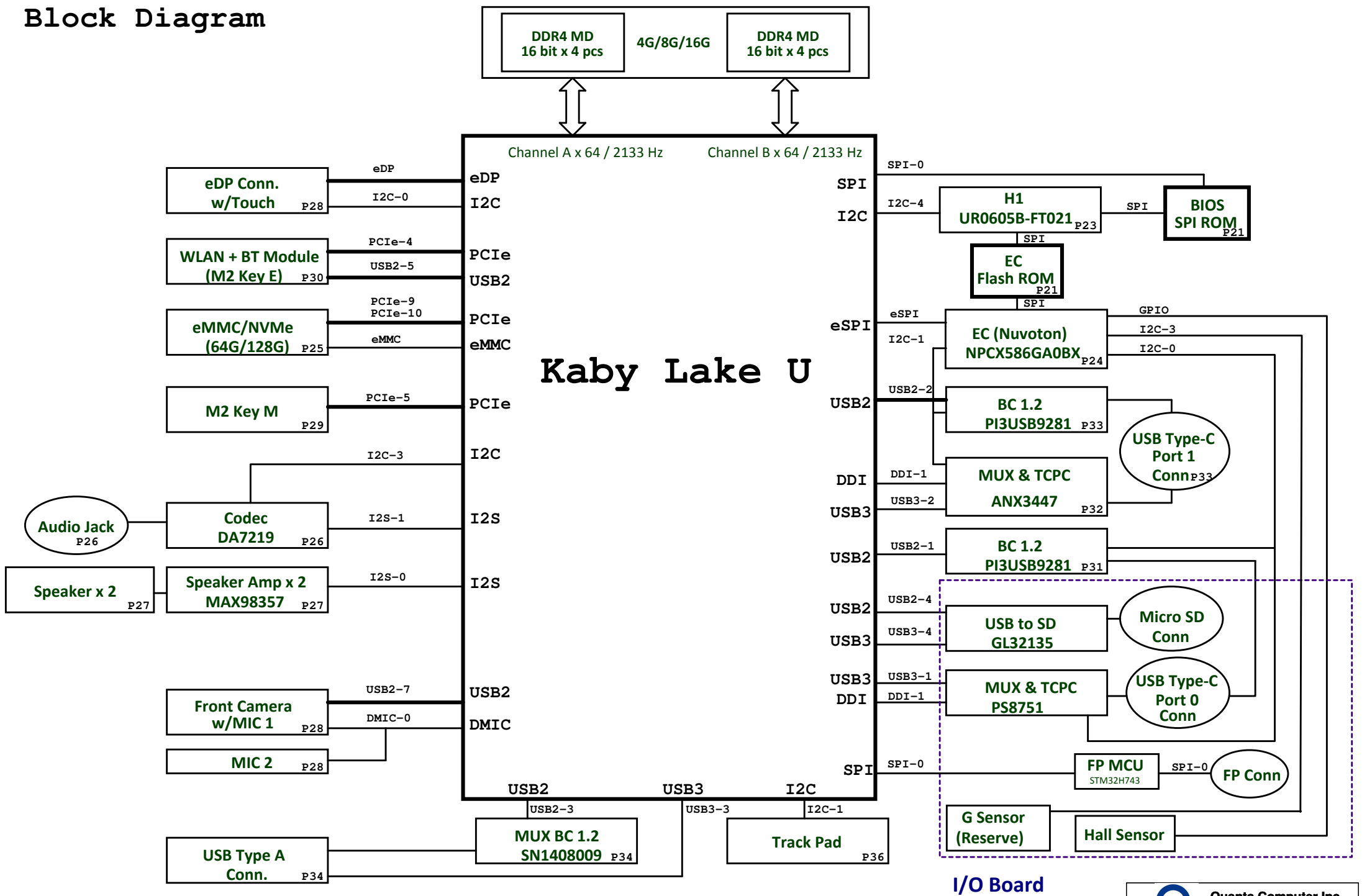
**Quanta Computer Inc.**

**PROJECT : ZAT**

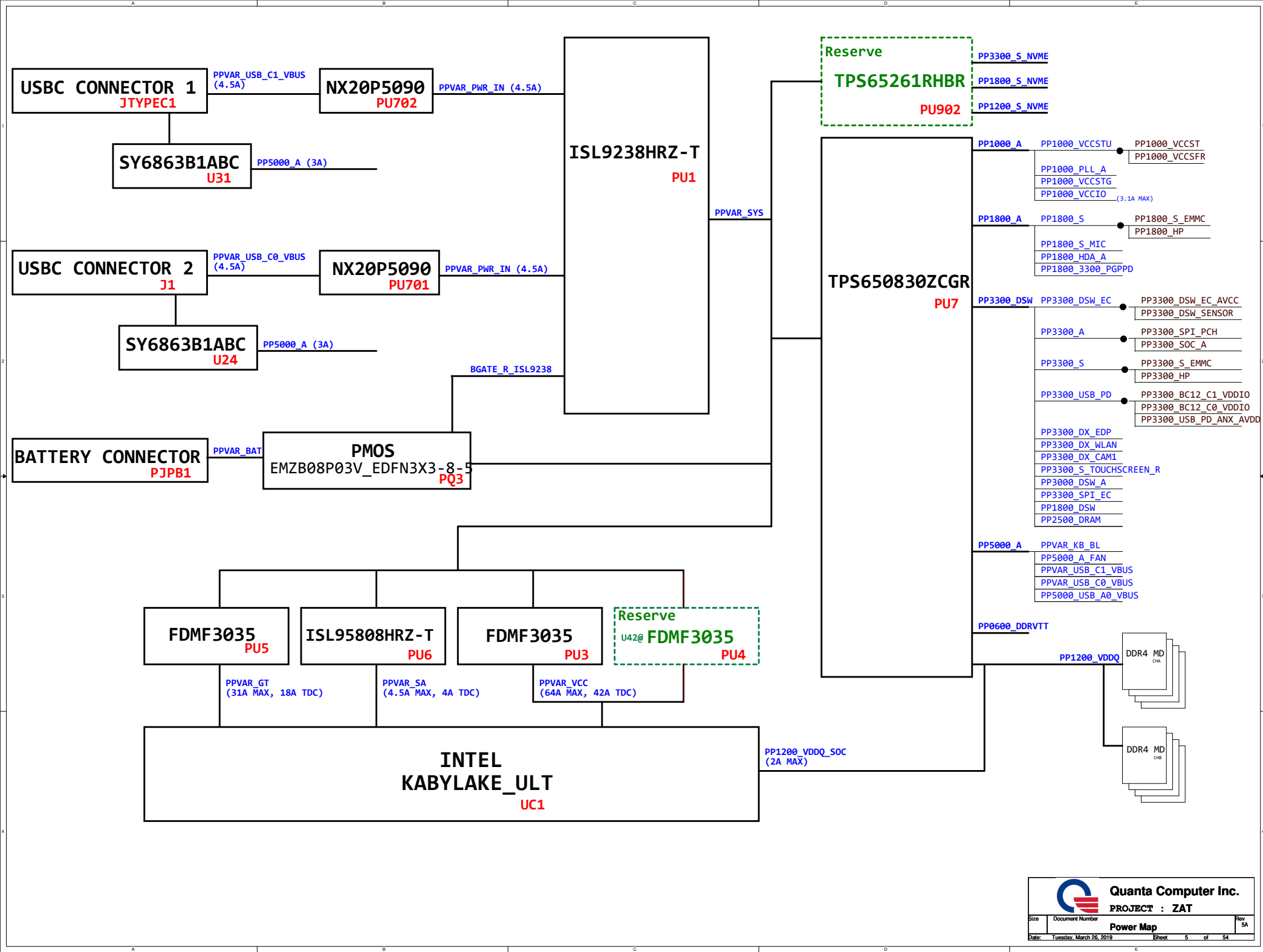
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		5A
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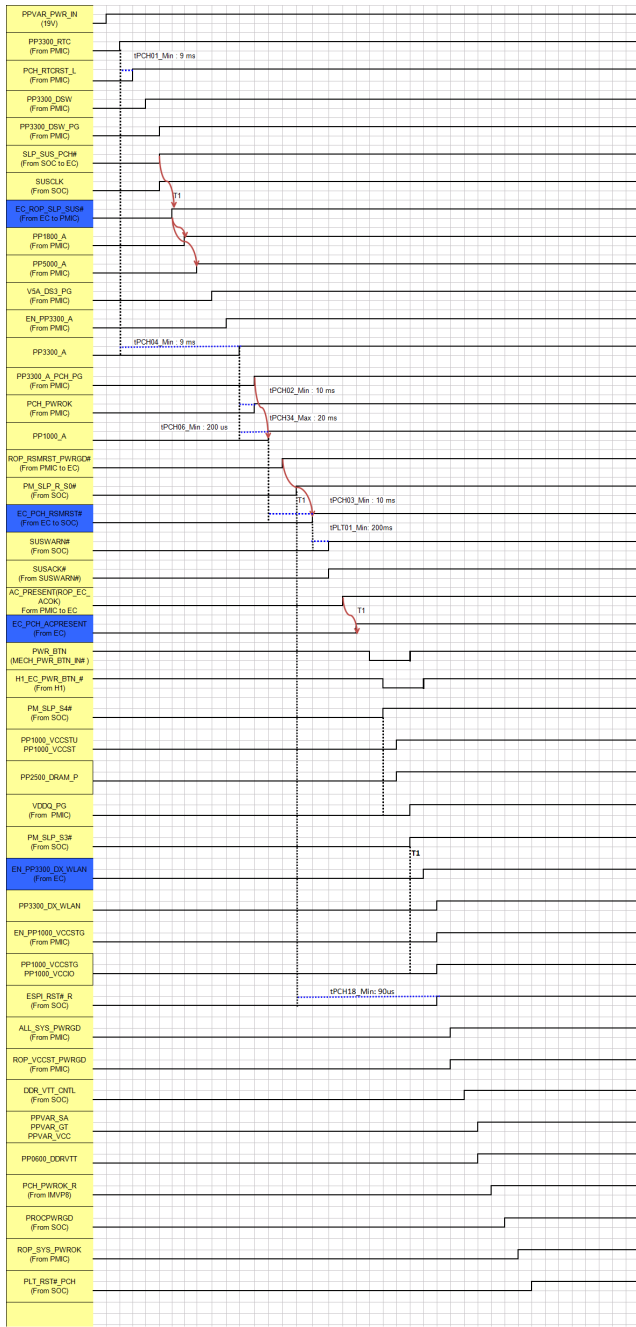
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Block Diagram





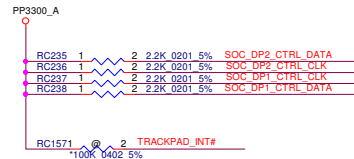




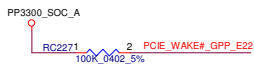


M/B SKU	Description	BOM stuff
31ZATMB0000	ZAT MB(CPUU22 C-3865 1.8/M8G/W32)UR118E1	U22@/XDP@/EMI@/INA@/ESPI@/ESD@/EMMC@/DSX_S01X@/DSX@/SDP@/NGFF@/CCD@/RF@
31ZATMB0010	ZAT MB(CPUU4213-8130 2.2H8GH32)1PUR118E1	U42@/XDP@/EMI@/INA@/ESPI@/ESD@/EMMC@/DSX_S01X@/DSX@/SDP@/NGFF@/CCD@/RF@
31ZATMB0020	ZAT MB(CPUU4215-8250 1.6M16GW128)UR118E1	U42@/XDP@/EMI@/INA@/ESPI@/ESD@/EMMC@/DSX_S01X@/DSX@/DDF@/NGFF@/CCD@/RF@
31ZATMB0030	ZAT MB(CPUU4215-8250 1.6/M16GH64)UR118E1	U42@/XDP@/EMI@/INA@/ESPI@/ESD@/EMMC@/DSX_S01X@/DSX@/DDF@/NGFF@/CCD@/RF@

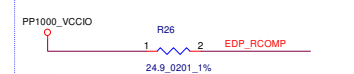
Vendor	Vendor P/N	Quanta P/N	Memory	Package	[3]	[2]	[1]	[0]	RAM ID			
TBD					0	0	0	0	R90	R91	R92	R93
Micro	MT40A256M16GE-083E	AKD5JGSTL26	4G	SDP	0	0	0	1	R90	R91	R92	R89
Samsung	K4A8G165WB-BCRC	AKD5QZ0T508	8G	SDP	0	0	1	0	R90	R91	R88	R93
Hynix	H5AN4G6NBJR-UHC	AKD5JGUTW01	4G	SDP	0	0	1	1	R90	R91	R88	R89
Hynix	H5ANAG6NAMR-UHC	AKD5RGUTW07	16G	DDP	0	1	0	0	R90	R87	R92	R93
Hynix	H5ANAG6NCMR-VKC	AKD5RGUTW08	16G	DDP	0	1	0	1	R90	R87	R92	R89
Hynix	H5AN8G6NAFR-UHC	AKD5QGSTW09	8G	SDP	0	1	1	0	R90	R87	R88	R93
Samsung	K4A4G165WE-BCRC	AKD5JGUT504	4G	SDP	0	1	1	1	R90	R87	R88	R89
Samsung	K4A8G165WC-BCTD	AKD5FGUT502	8G	SDP	1	0	0	0	R86	R91	R92	R93
Hynix	H5AN4G6NAFR-UHC	AKD5JGUTW03	4G	SDP	1	0	0	1	R86	R91	R92	R89
TBD					1	0	1	0	R86	R91	R88	R93
TBD					1	0	1	1	R86	R91	R88	R89
Samsung	K4AAG165WB-MCRC	AKD5LGUT500	16G	DDP	1	1	0	0	R86	R87	R92	R93
Micro	MT40A1G16KNR-075:E	AKD5MZSTL04	16G	DDP	1	1	0	1	R86	R87	R92	R89
Micro	MT40A512M16LY-075E	AKD5LZSTL25	8G	SDP	1	1	1	0	R86	R87	R88	R93
Hynix	H5AN8G6NCJR-VKC	AKD5QGSTW14	8G	SDP	1	1	1	1	R86	R87	R88	R89



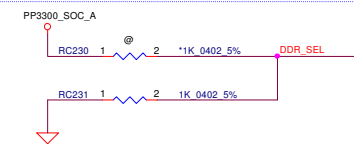
DDI1 for USB-C (M/B)



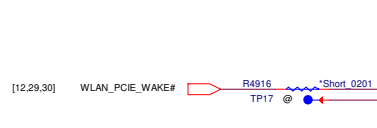
DDI2 for USB-C (Sub/B)



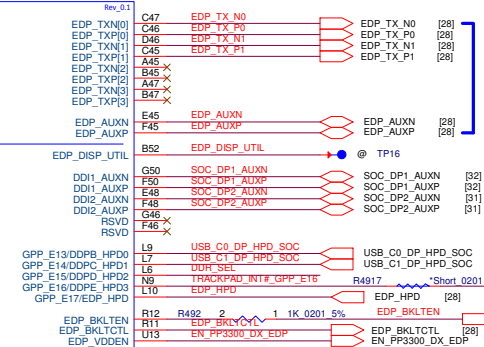
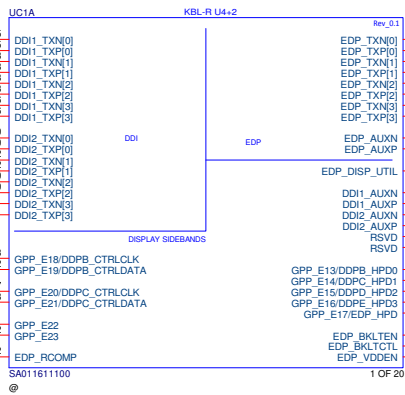
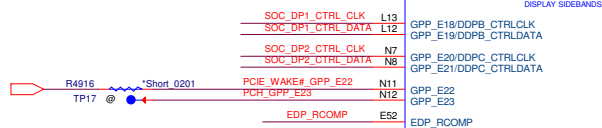
Trace width = 20 mils, Spacing = 25mil, Max length = 100mils



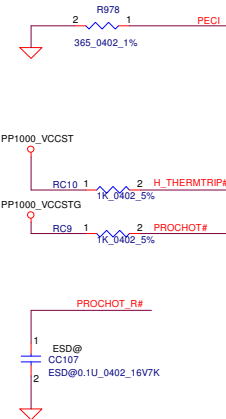
DDR\_SEL : DDR4 (RC231) ; LPDDR3 (RC230).  
Nami default support DDR4.



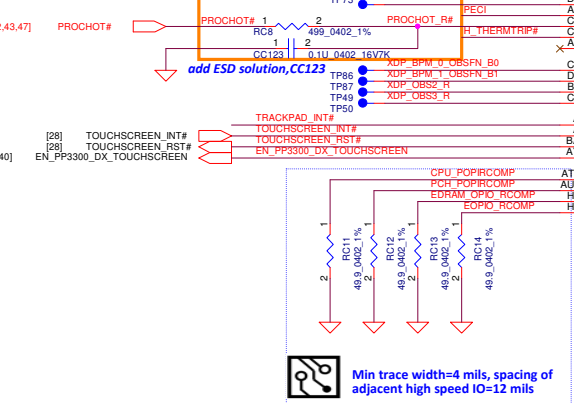
[12.29.30] WLAN\_PCIE\_WAKE#



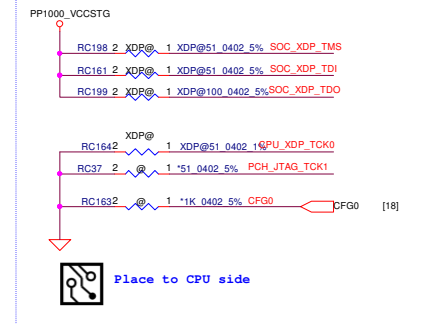
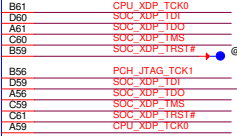
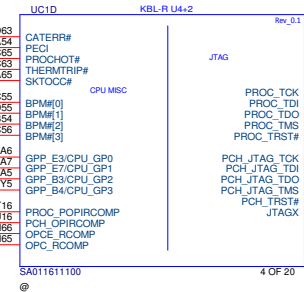
Remove  
EDP\_TX\_N3/EDP\_TX\_N2/  
EDP\_TX\_P3/EDP\_TX\_P2



[22.24.42.43.47] PROCHOT#



Min trace width=4 mils, spacing of adjacent high speed IO=12 mils



Place to CPU side



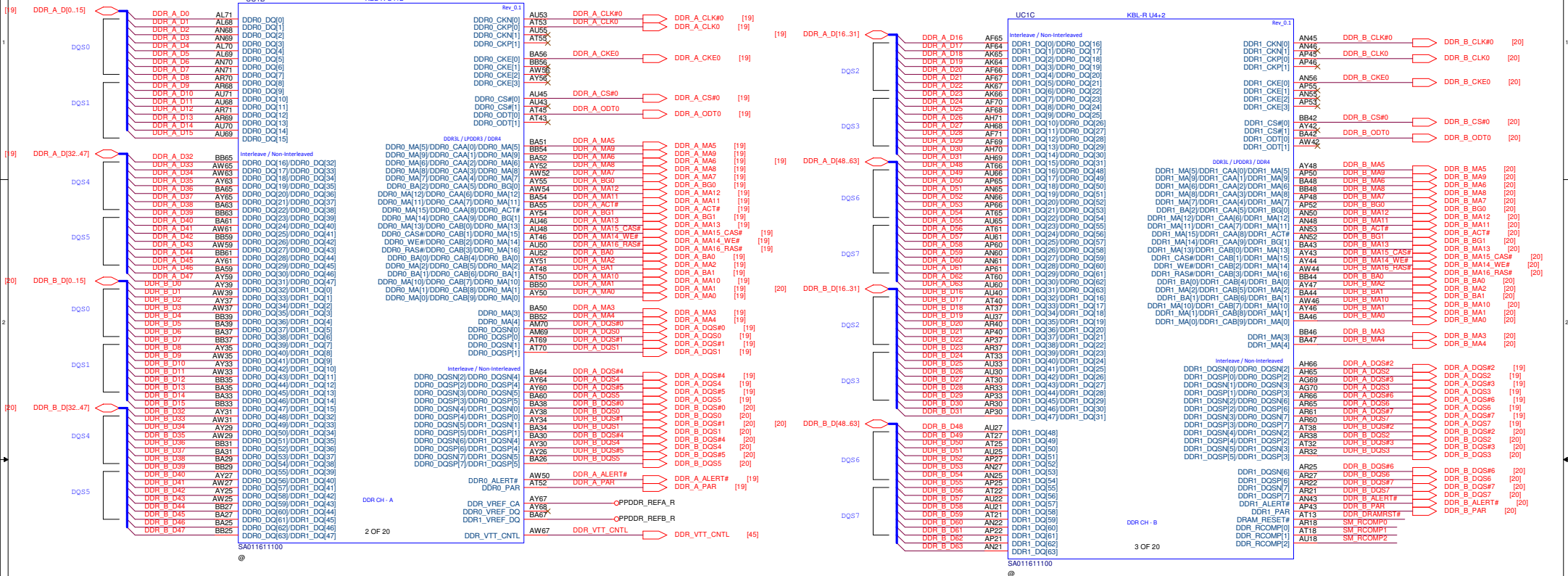
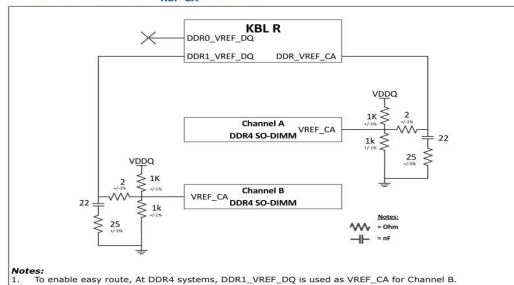
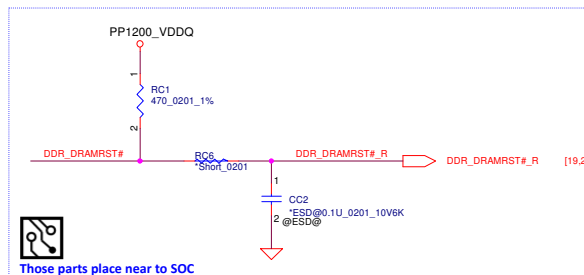


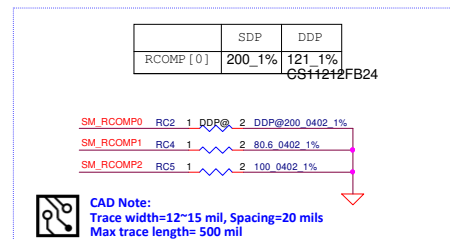
Figure 4-16. KBL R DDR4 SODIMM VREF-CA Overview



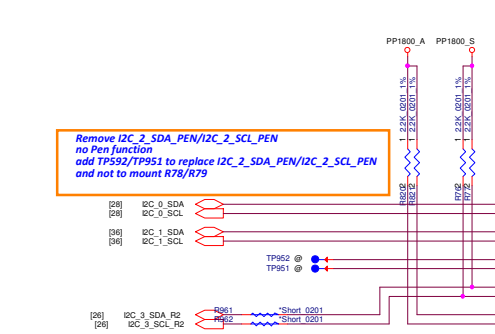
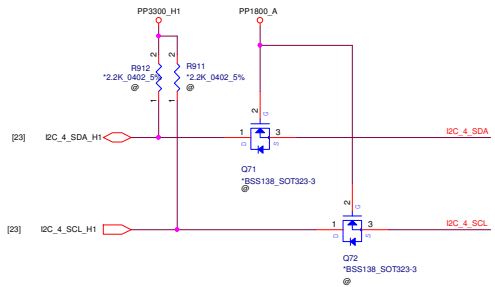
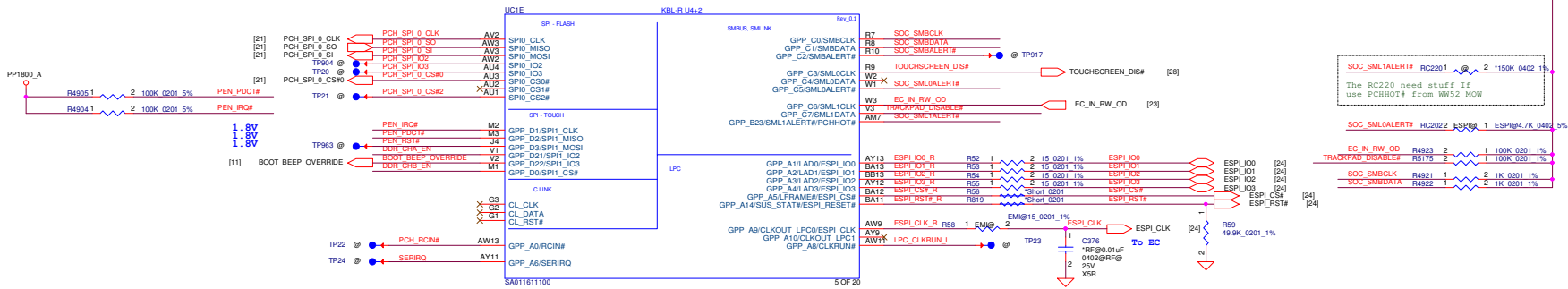
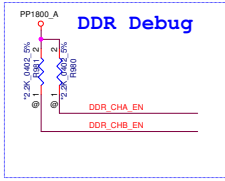
Notes:  
1. To enable easy route, At DDR4 systems, DDR1\_VREF\_DQ is used as VREF\_CA for Channel B.



Those parts place near to SOC



CAD Note:  
Trace width=12~15 mil, Spacing=20 mil  
Max trace length= 500 mil



Remove I2C\_2\_SDA\_PEN/I2C\_2\_SCL\_PEN  
no pen function  
add TP592/TP951 to replace I2C\_2\_SDA\_PEN/I2C\_2\_SCL\_PEN  
and not to mount R78/R79

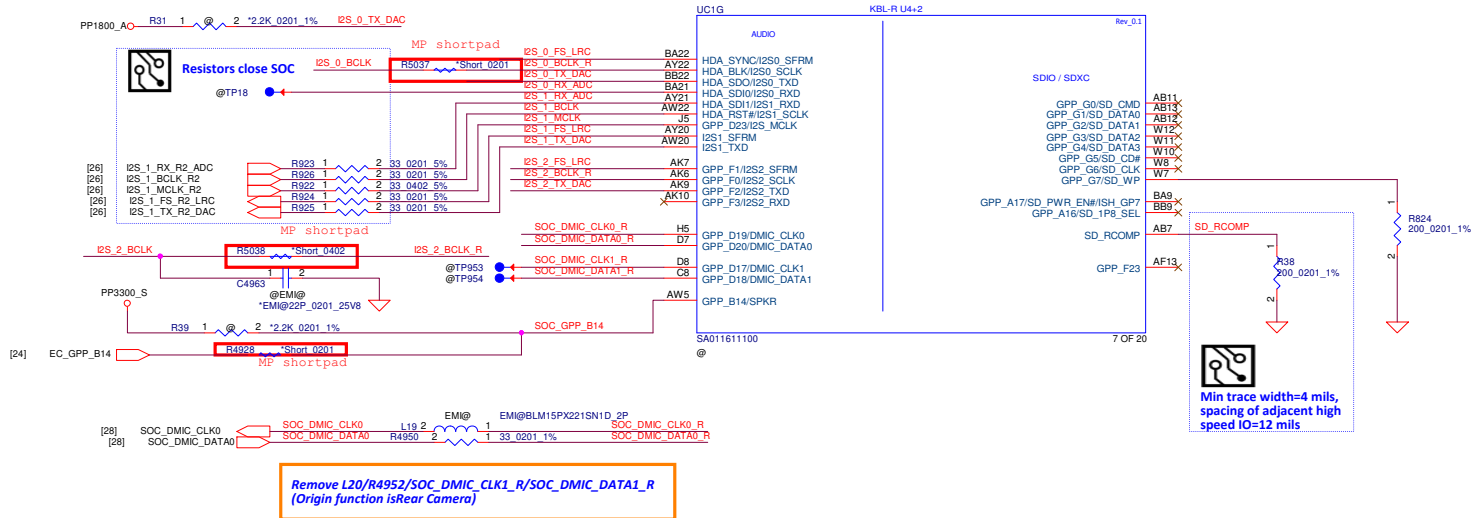
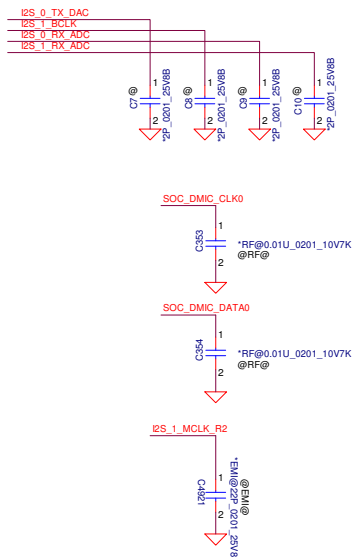
I2C Bus	Function	Bus Voltage	Module Voltage
I2C_0	Touch Screen	3.3V	3.3V
I2C_1	Track Pad	3.3V	3.3V
I2C_2	PEN	1.8V	1.8V
I2C_3	HP AMP	1.8V	1.8V
I2C_4	N/A	1.8V	N/A

PIN	FUNCTION	INTENT
GPP_B23/SML1ALERT#	IPD = EXI BOOT STALL BYPASS DISABLE PU = EXI BOOT STALL BYPASS ENABLED	DISABLE
GPP_B18/GSPI0_MOSI	IPD = DISABLE NO REBOOT MODE PU = ENABLE NO REBOOT MODE	DISABLE
GPP_C2/SMBALERT#	IPD = DISABLE TLS CONFIDENTIALITY PU = ENABLE TLS CONFIDENTIALITY	DISABLE
GPP_B22/GSPI1_MOSI	IPD = BOOT FROM SPI PU = BOOT FROM LPC	SPI
GPP_C5/SML0ALERT#	IPD = LPC IS SELECTED FOR EC PU = ESPI IS SELECTED FOR EC	ESPI

STRAPS ON THIS PAGE

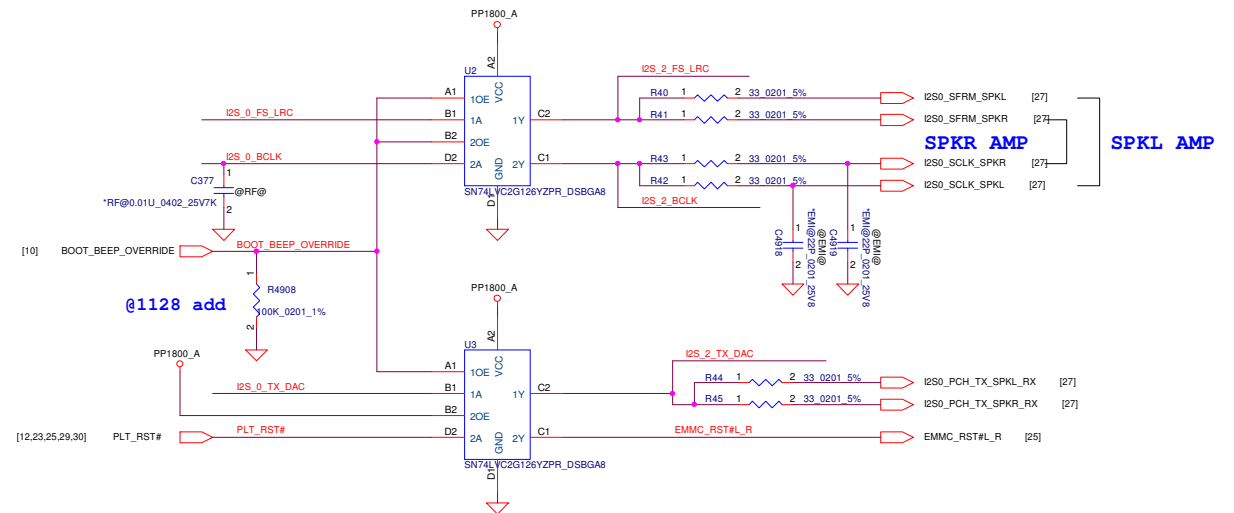
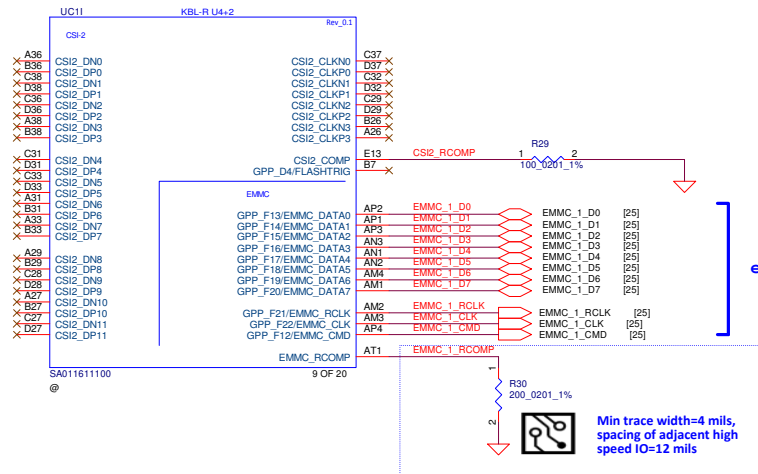
PIN	FUNCTION	INTENT
GPP_E19/DDPB_CTRLDATA	IPD = DO NOT DETECT PORT B PU = DETECT PORT B	DETECT PORT B
GPP_E21/DDPC_CTRLDATA	IPD = DO NOT DETECT PORT C PU = DETECT PORT C	DETECT PORT C

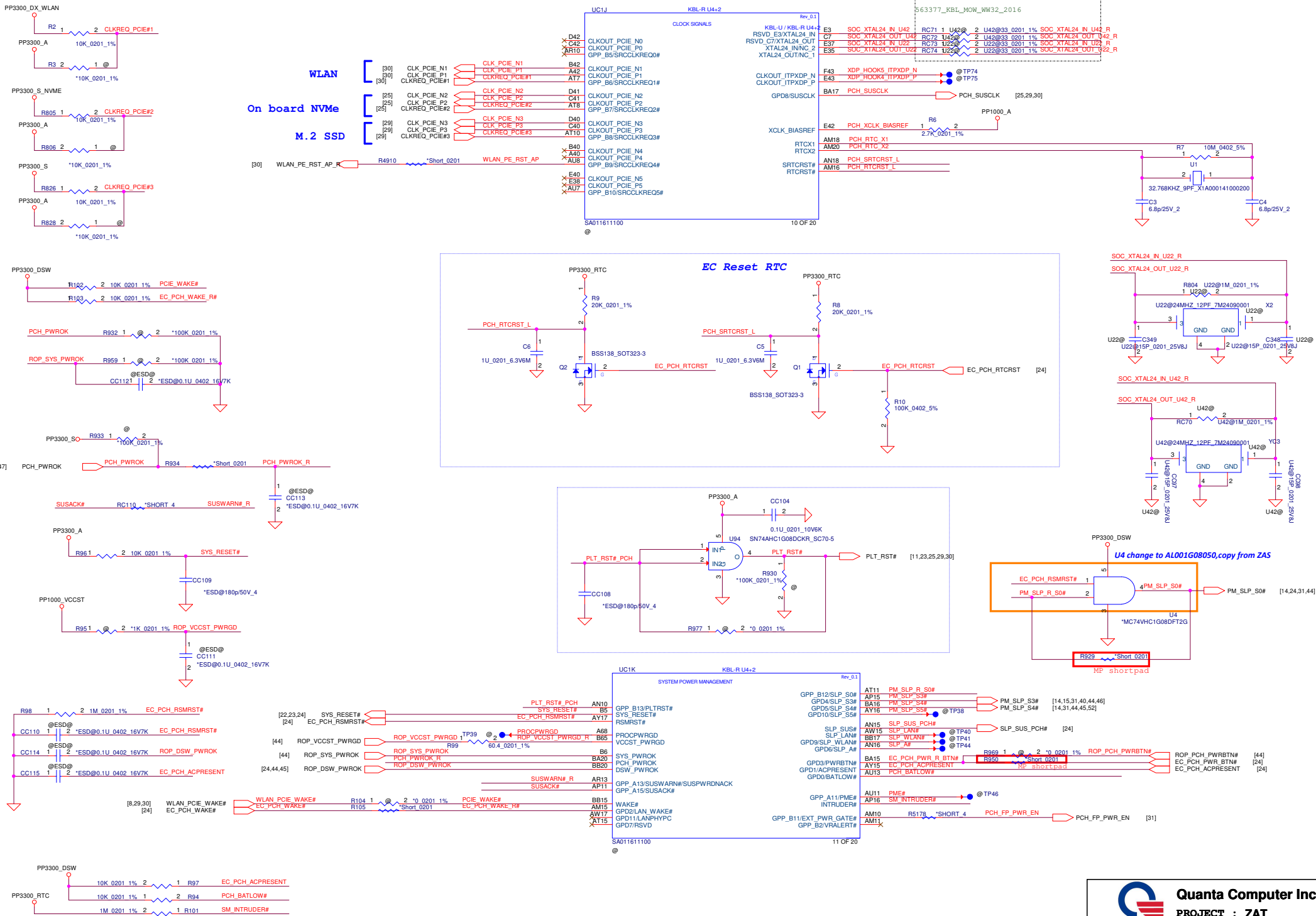
STRAPS ON THIS PAGE



## STRAPS ON THIS PAGE

PIN	FUNCTION	INTENT
PCH_BUZZER	IPD = DISABLE TOP SWAP OVERRIDE PU = ENABLE TOP SWAP OVERRIDE	DISABLE
HDA_SDO/I2S_TXD0	IPD = ENABLE DESCRIPTOR SECURITY PU = DISABLE DESCRIPTOR SECURITY	ENABLE

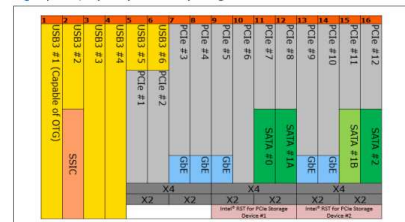




NGFF WLAN+BT (Key E)

M.2 (TBD)

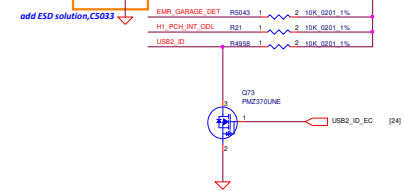
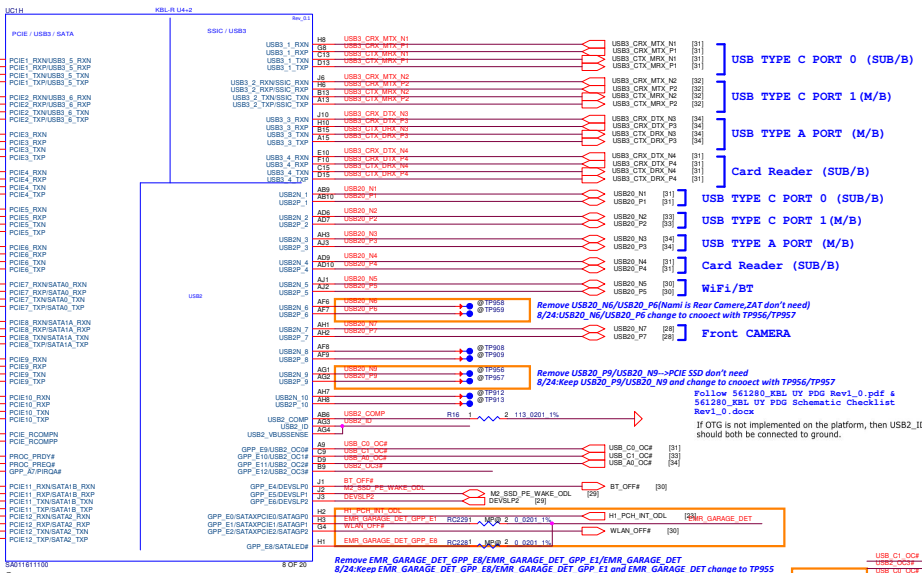
On board NVMe



- The 16 HSIO lanes on KBL R U PCH-LP supports the following configurations:
- Up to 12 PCIe\* lanes (multiplexed with USB 3.0 lanes, SATA lanes)
    - Only a maximum of 6 PCIe\* Root Ports (or devices) can be enabled at any time
    - PCIe\* Lanes 1-4, 5-8, and 9-12 each can be individually configured as 4x1, 2x2, 1x2+2x1, 2x1+1x2, or 1x4
  - Up to 3 SATA lanes (multiplexed with PCIe\* lanes)
    - SATA lane 1 has the flexibility to be mapped to either PCIe\* lane 8 or 11
  - Up to 6 USB 3.0 lanes (multiplexed with PCIe\* lanes)
    - On-the-go (OTG) capability is available on USB 3.0 lane 1
    - One SSIC v1 lane is multiplexed with USB 3.0 lane 2
  - One GBE device
    - GBE can be mapped into one of the PCIe\* lanes 3-5 and 9-10
    - When GBE is enabled, there can be at most up to 5 PCIe\* Root Ports (or devices) enabled
  - Up to 2 Intel® RST for PCIe\* Storage Devices
    - Each device can be x2 or x4 and can be implemented on either PCIe\* lanes 5-8 or 9-12
  - For unused SATA/PCIe\* Combo Lanes, Flex I/O Lanes that can be configured as PCIe\* or SATA, the lanes must be statically assigned to SATA or PCIe\* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool. These unused SATA/PCIe\* Combo Lanes must not be assigned as polarity based.

Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U / Base-U with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe / USB 3.0	PCIe / LAN	PCIe / LAN	PCIe / LAN	PCIe / LAN	SATA	SATA	PCIe / LAN	PCIe / LAN	PCIe / SATA	PCIe / SATA
Premium-U / Premium-U with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe / USB 3.0	PCIe / LAN	PCIe / LAN	PCIe / LAN	PCIe / LAN	PCIe / SATA	PCIe / SATA	PCIe / LAN	PCIe / LAN	PCIe / SATA	PCIe / SATA
Premium-Y / Premium-Y with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe / USB 3.0	PCIe / LAN	PCIe / LAN	PCIe / LAN	PCIe / LAN	PCIe / SATA	PCIe / SATA	PCIe / LAN	PCIe / LAN	N/A	N/A

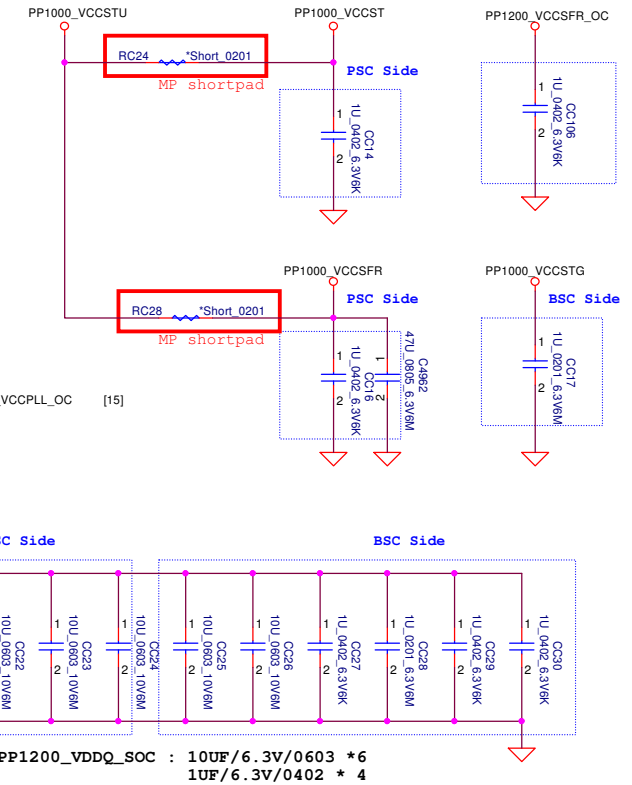


The schematic diagram illustrates the internal circuitry of the PP1800 A to PP1800 S power supply module. It features two input sections at the top: PP5000\_A and PP1000\_A, both providing +1.0V\_VCCSTU. These inputs are connected through capacitors CC4 and CC5 (1µF, 0402, 6.3V6K) to the VIN1 pin of the UC4 controller. The UC4 controller also receives EN\_PP1000\_VCCSTU and EN\_PP1800\_S signals. Its output VOUT1 is connected to the SS1 pin of the J7110DFNC-TRPBF converter, which is powered by PP1000\_VCCSTU through capacitor CC6 (10P, 0402, 50VB). The converter's other input is connected to PP1800\_A through capacitor CC9 (1µF, 0402, 6.3V6K). The converter's output VOUT2 provides the final output voltage, regulated by feedback from PP1800\_S through capacitor CC10 (10P, 0402, 25V6). The module includes thermal pads for heat dissipation.

**I (Max) : 0.04 A (+1.0V\_VCCSTU)**  
**RON (Max) : 25 mohm**  
**V drop : 0.001 V**

**I (Max) : 0.536 A (+1.8VS)**  
**RON (Max) : 25 mohm**  
**V drop : 0.013 V**

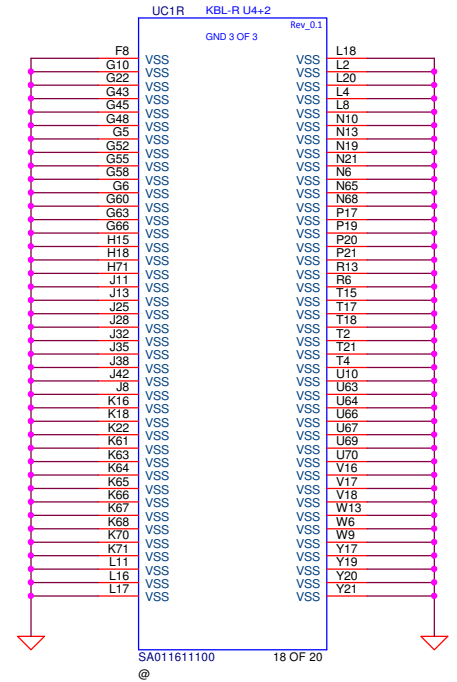
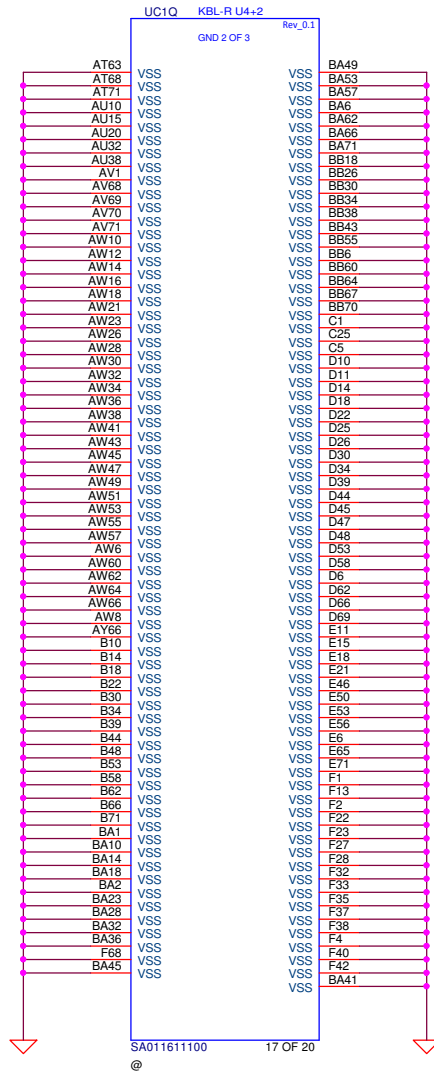
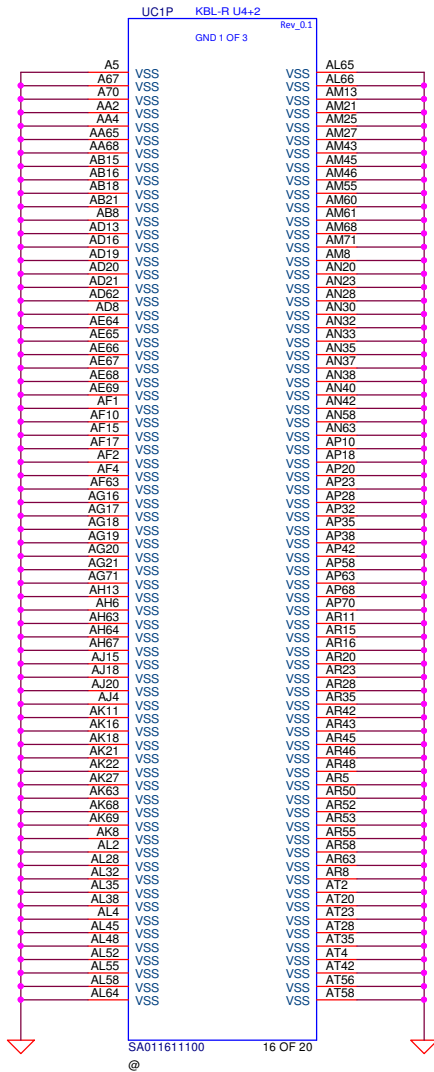
**PP1800 A TO PP1800 S**

[illegible][illegible]

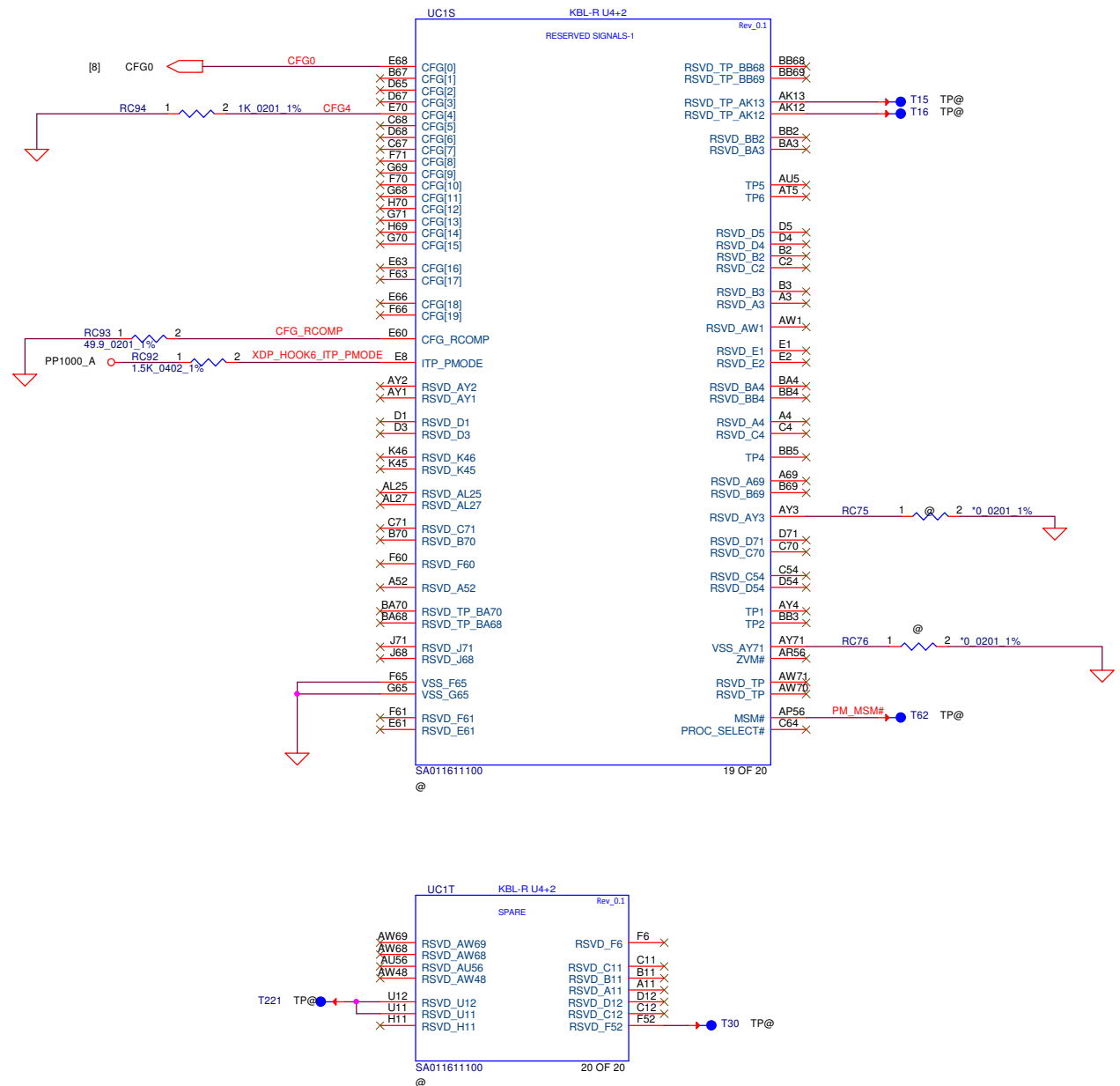




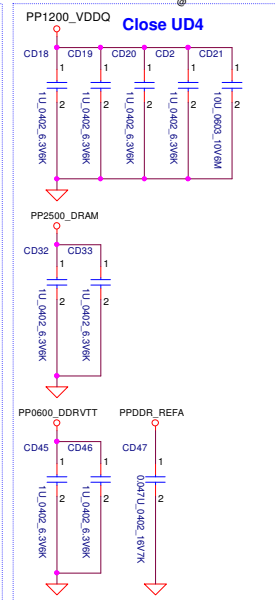
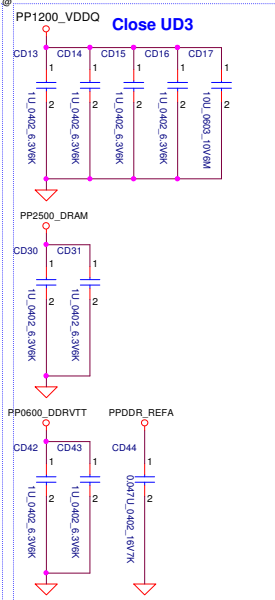
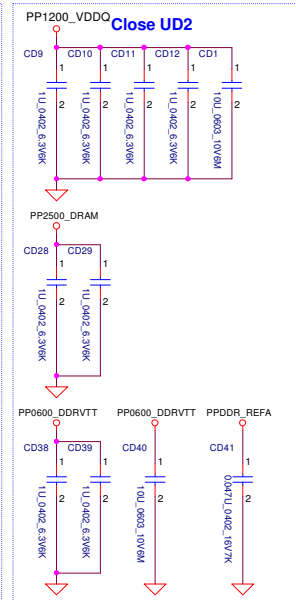
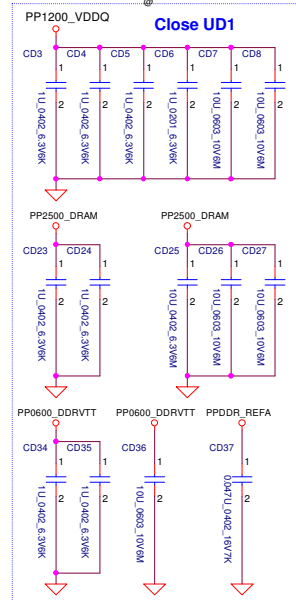
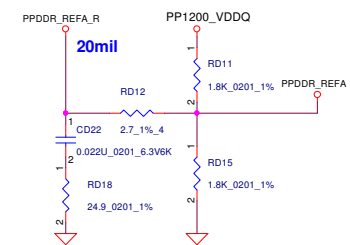
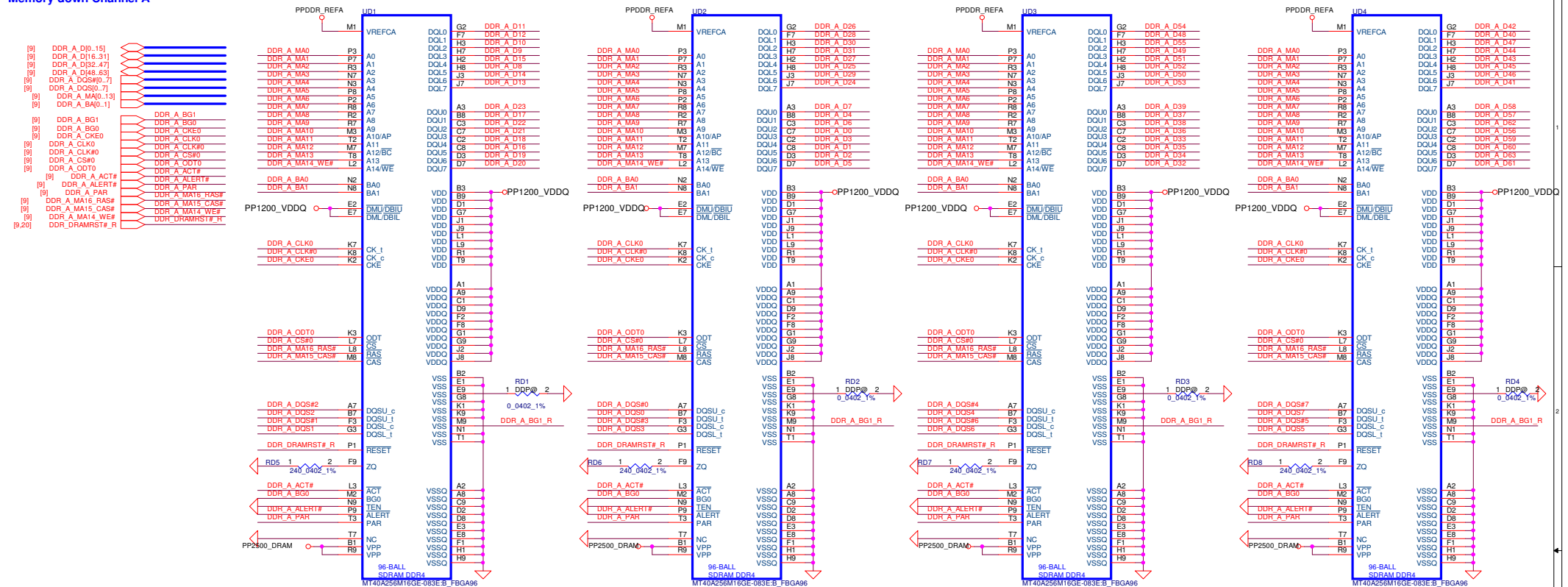




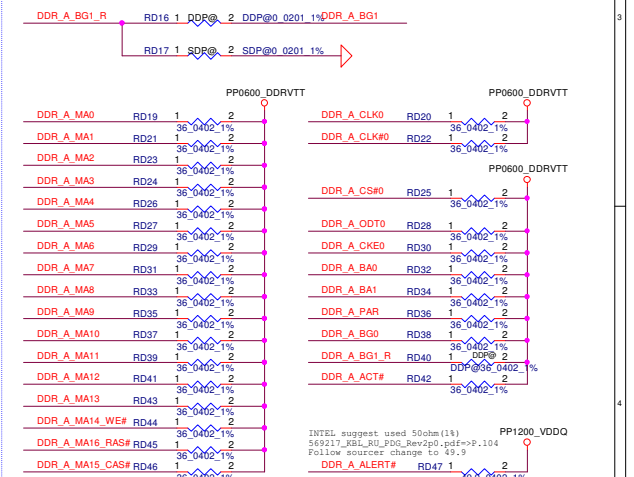
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



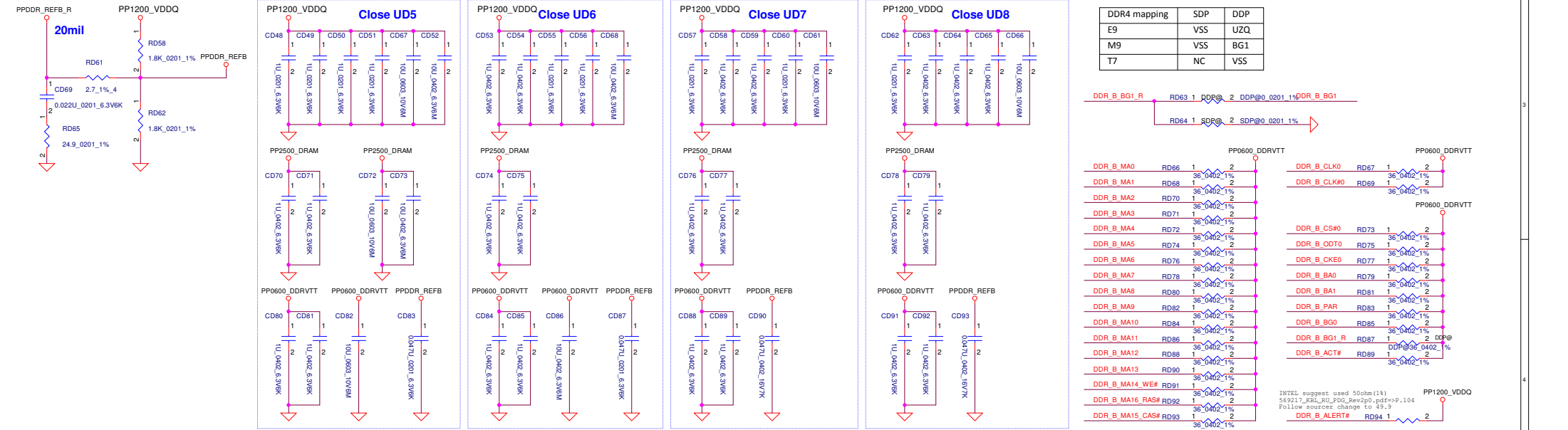
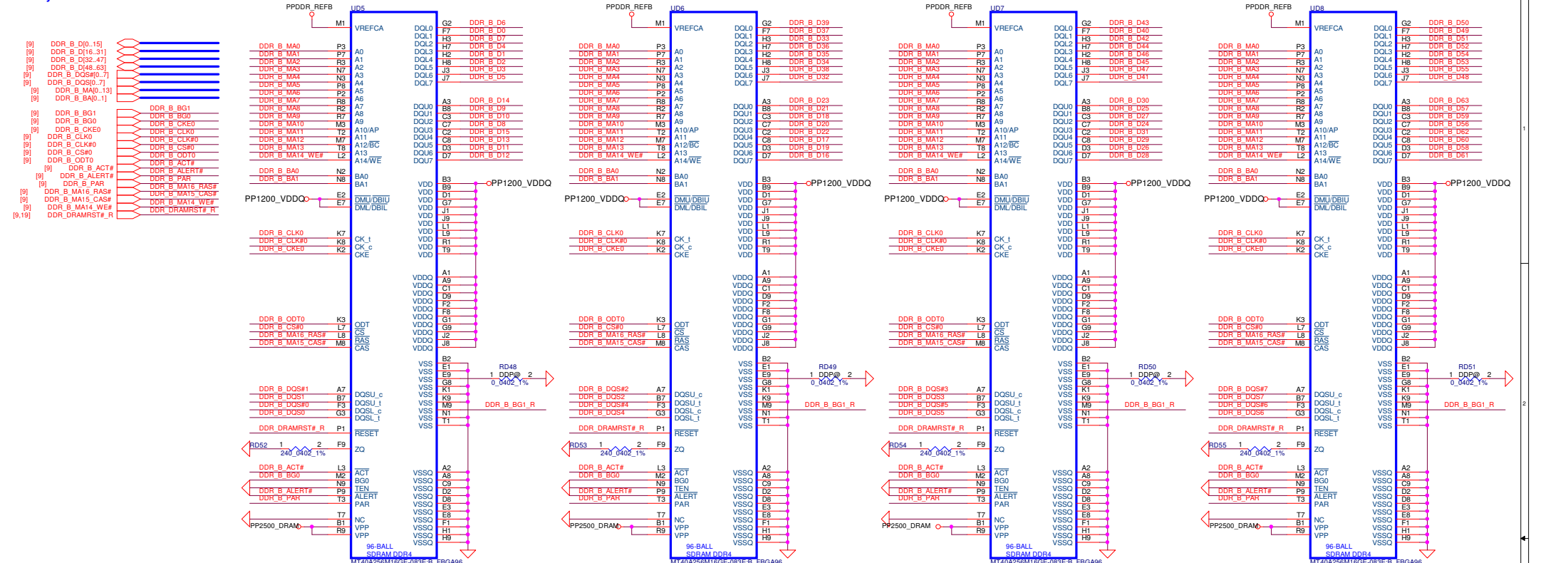
### Memory down Channel A



DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS



# Memory down Channel B

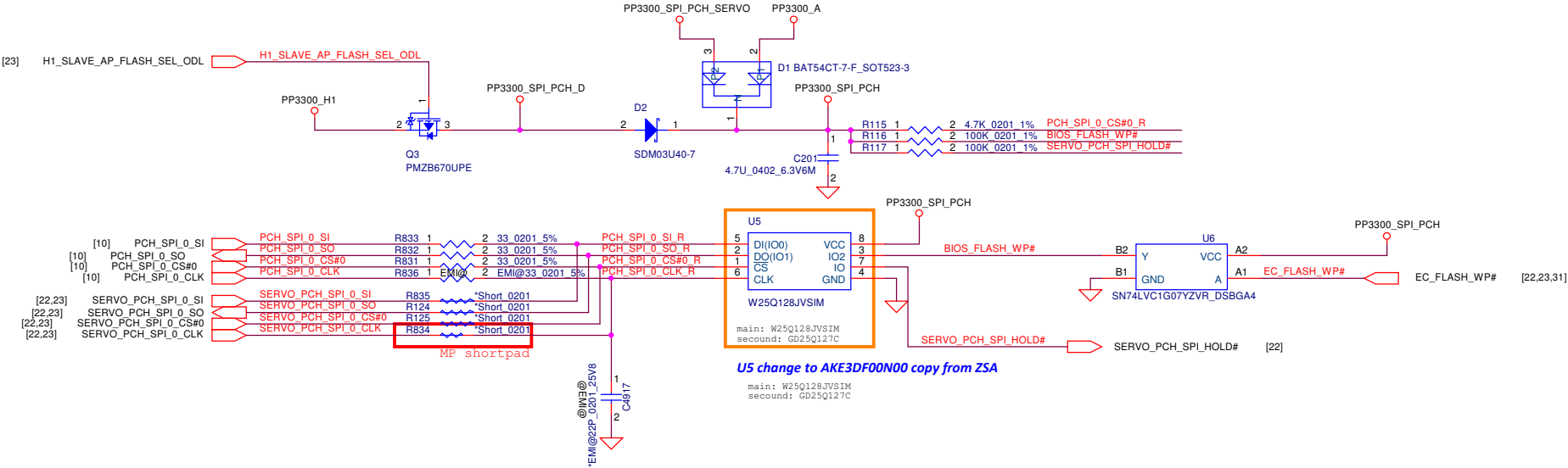


DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS

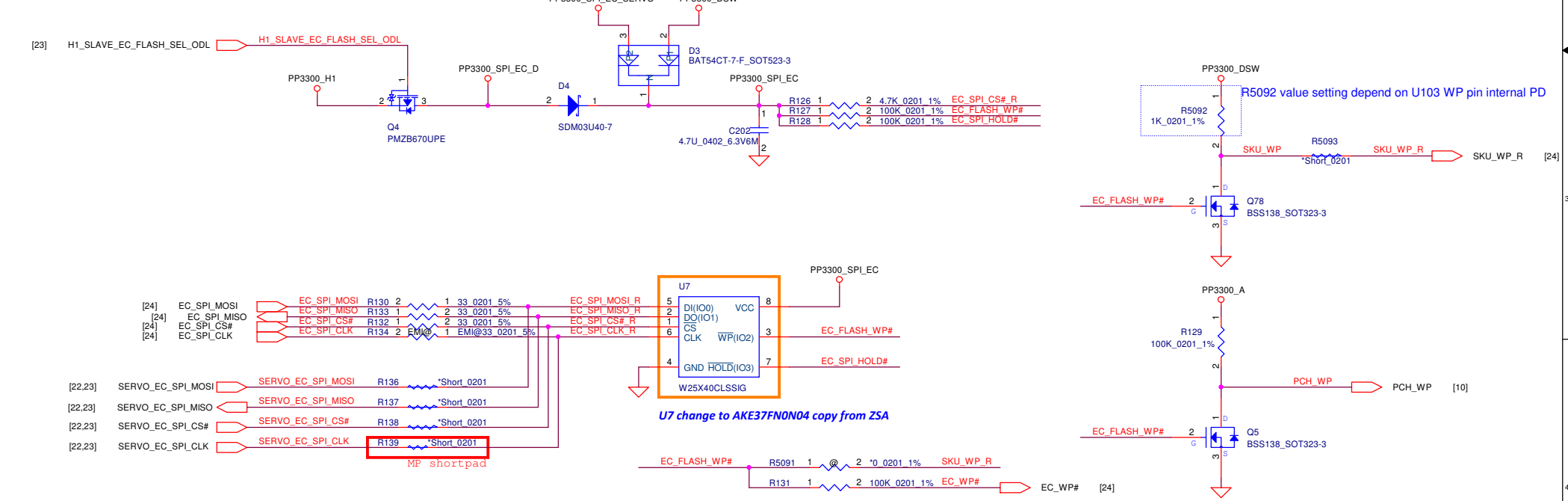
INTEL suggest used 50ohm(1k)  
569217\_KBL\_R01\_P00\_R00\_R00.pdf>P.104  
Follow sourcer change to 49.9  
DDR\_B\_ALERT# RD94 1 2 36 0402 1%  
49.9 0201 1%  
PP1200\_VDDQ



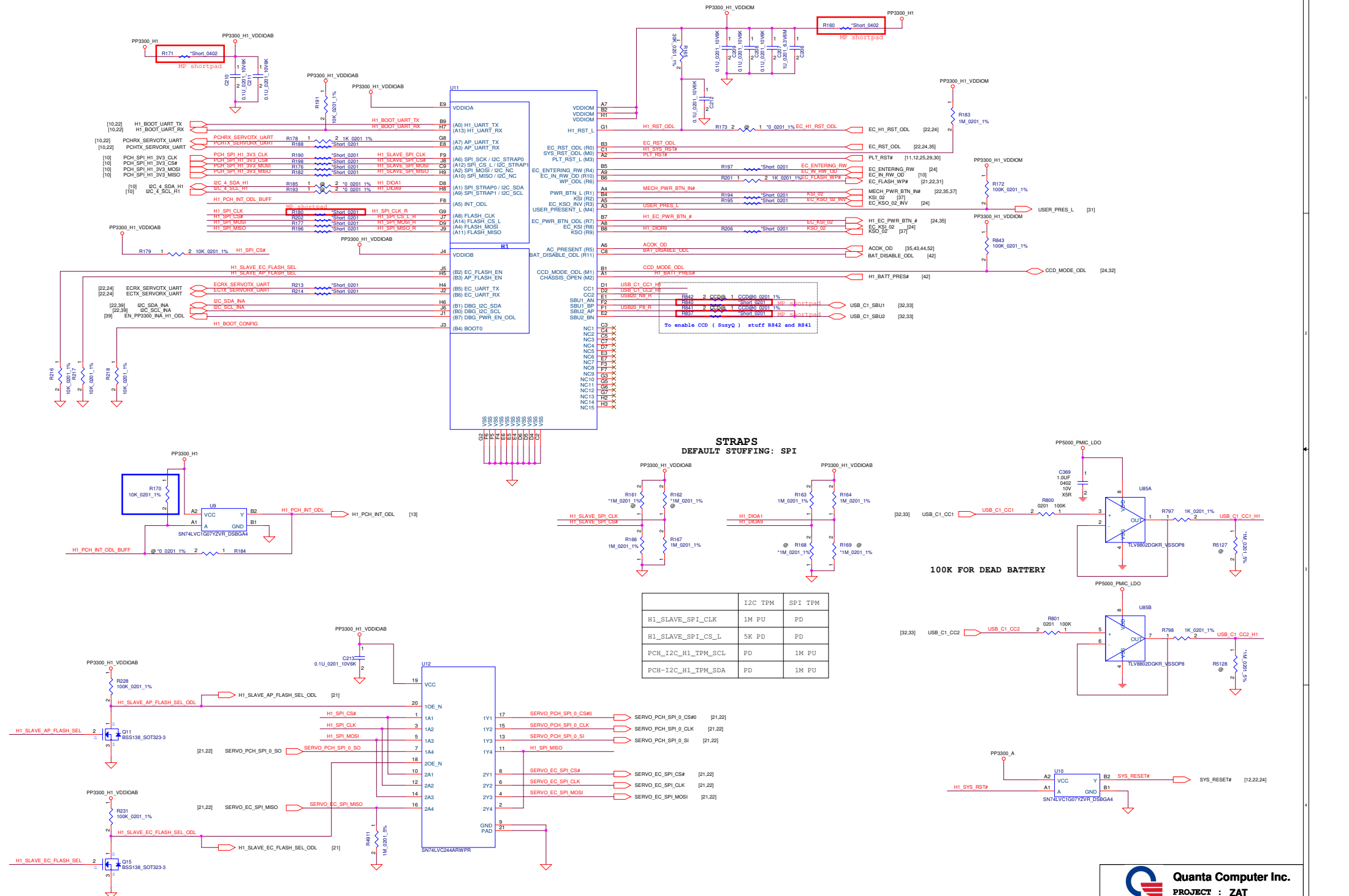
PCH SPI FLASH



EC FLASH ROM







### STRAPS DEFAULT STUFFING: SPI

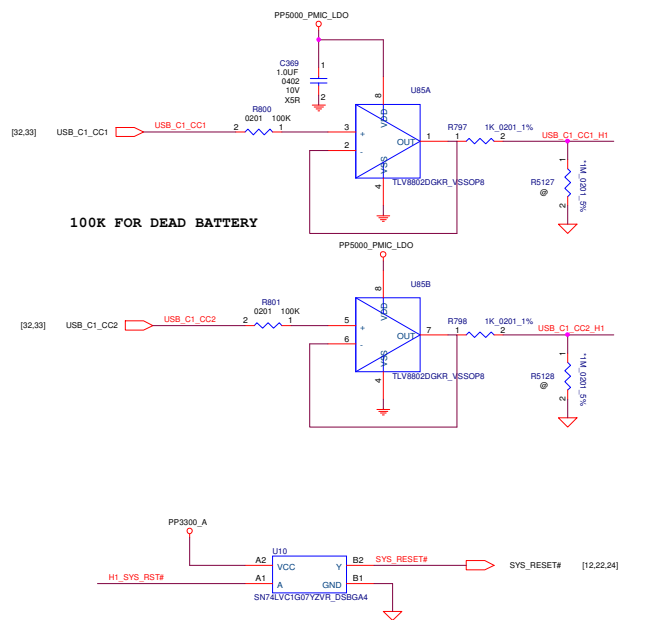
	I2C TPM	SPI TPM
H1_SLAVE_SPI_CLK	1M PU	PD
H1_SLAVE_SPI_CS_L	5K PD	PD
PCH_I2C_H1_TPM_SCL	PD	1M PU
PCH-I2C_H1_TPM_SDA	PD	1M PU

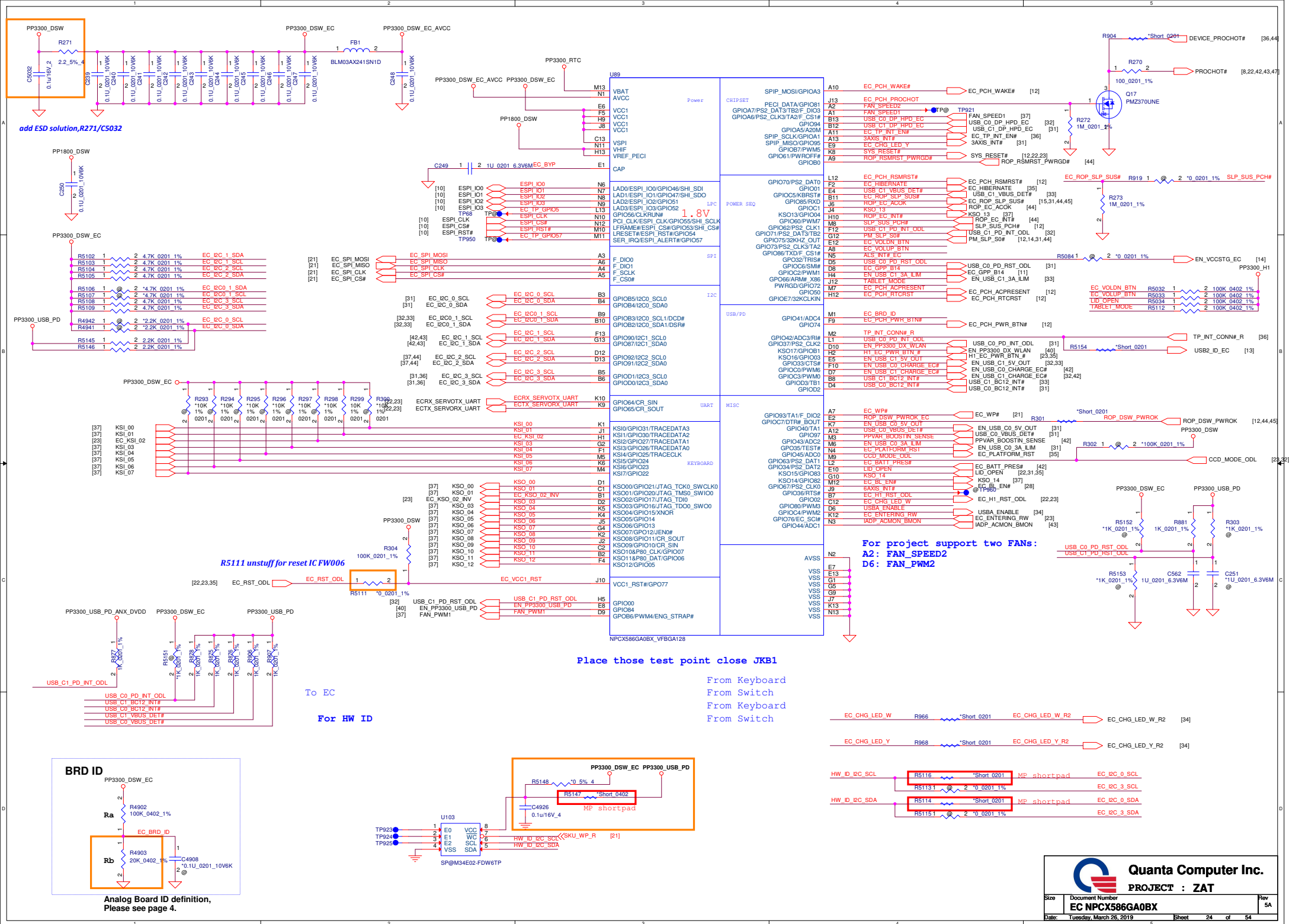
H1\_SLAVE\_SPI\_CLK

H1\_SLAVE\_SPI\_CS#

H1\_DIOA1

H1\_DIOA3



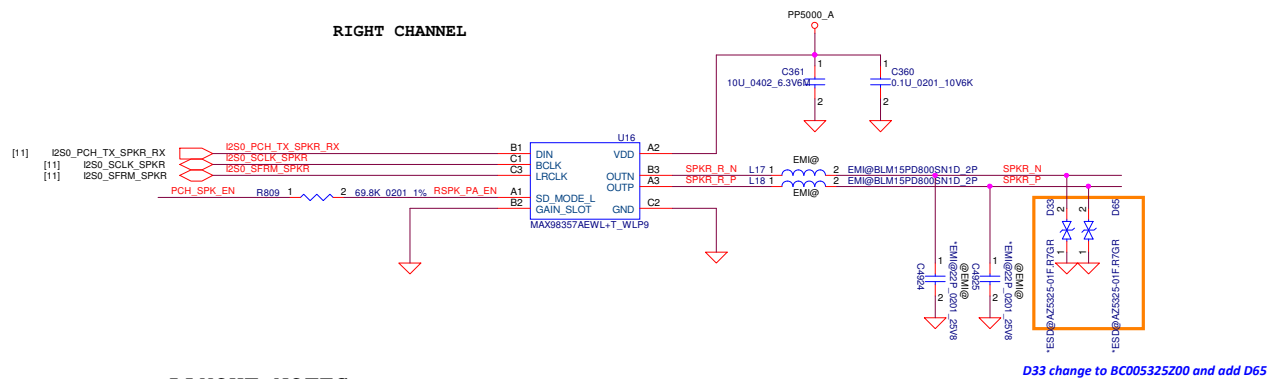
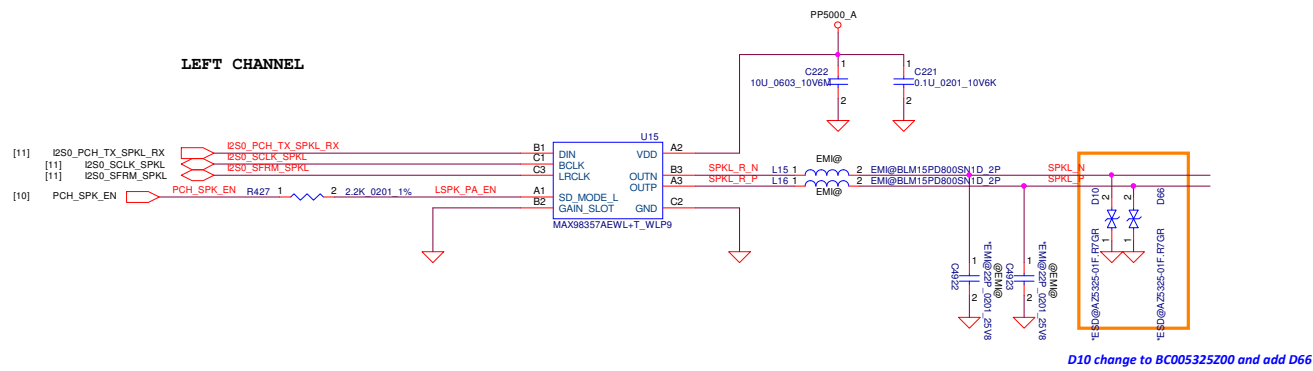








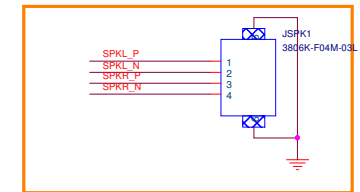
SPEAKER AMP



LAYOUT NOTES

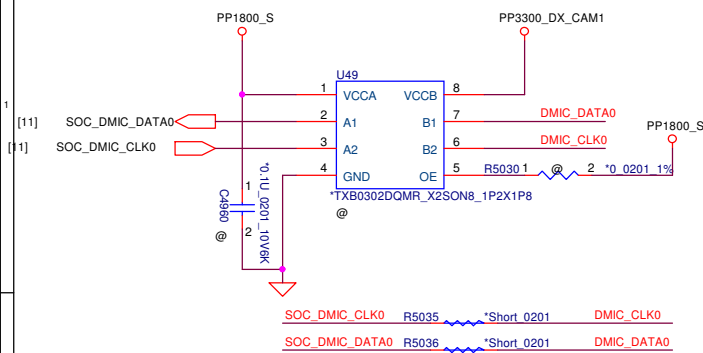
SPKL\_P, SPKL\_N & SPKR\_P, SPKR\_N SHOULD BE CONNECTED AS CLOSE TO THE SPEAKER CONNECTOR AS POSSIBLE

SPEAKER CONNECTOR



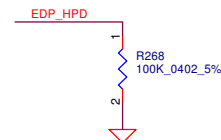
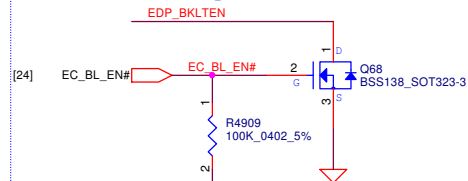
JHSPK1 copy from ZSA(Same P/N, FP change to wtb-50278-00401-v01-4p-1)

## Reserve for DMIC data/clock 3.3V

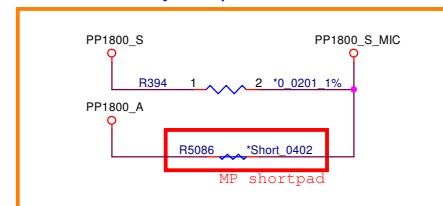


Default for DMIC data/clock 1.8V

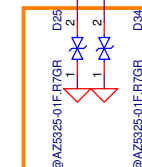
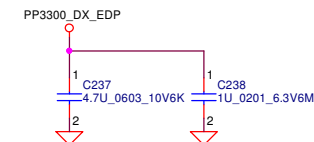
## LCD Backlight control from EC



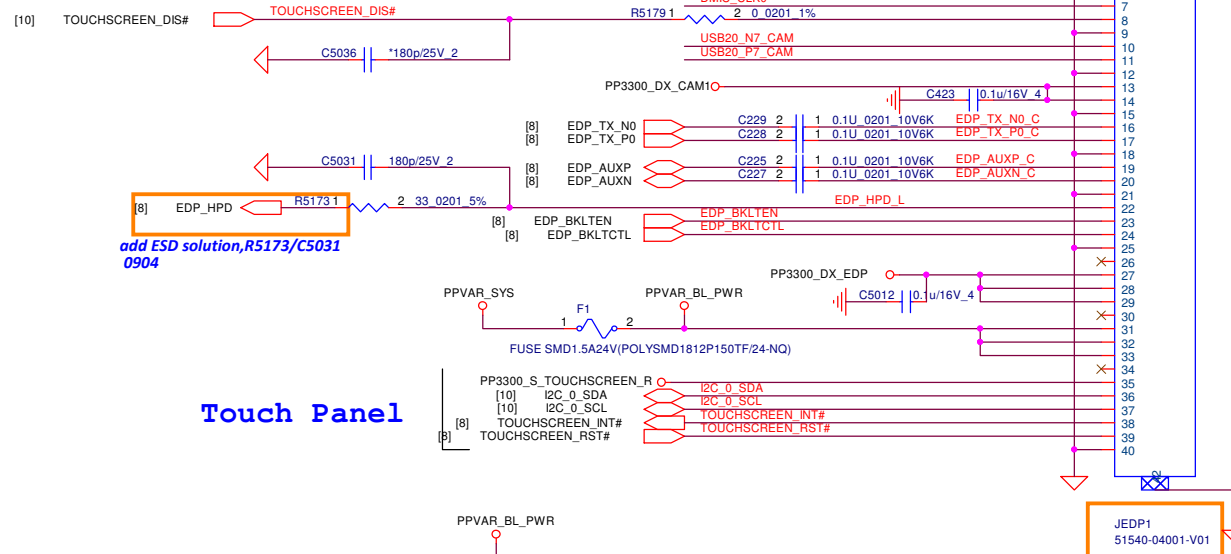
*add R5086 for MIC power rail*



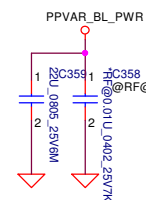
Current rating 0.5A@pin



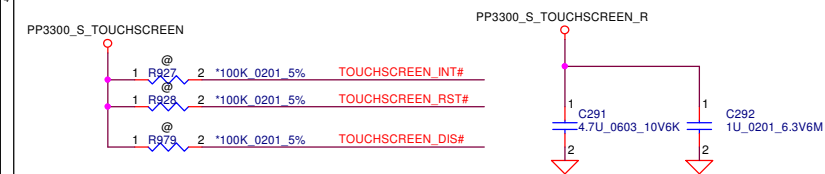
**D34 change to BC005325Z00 and add D25**



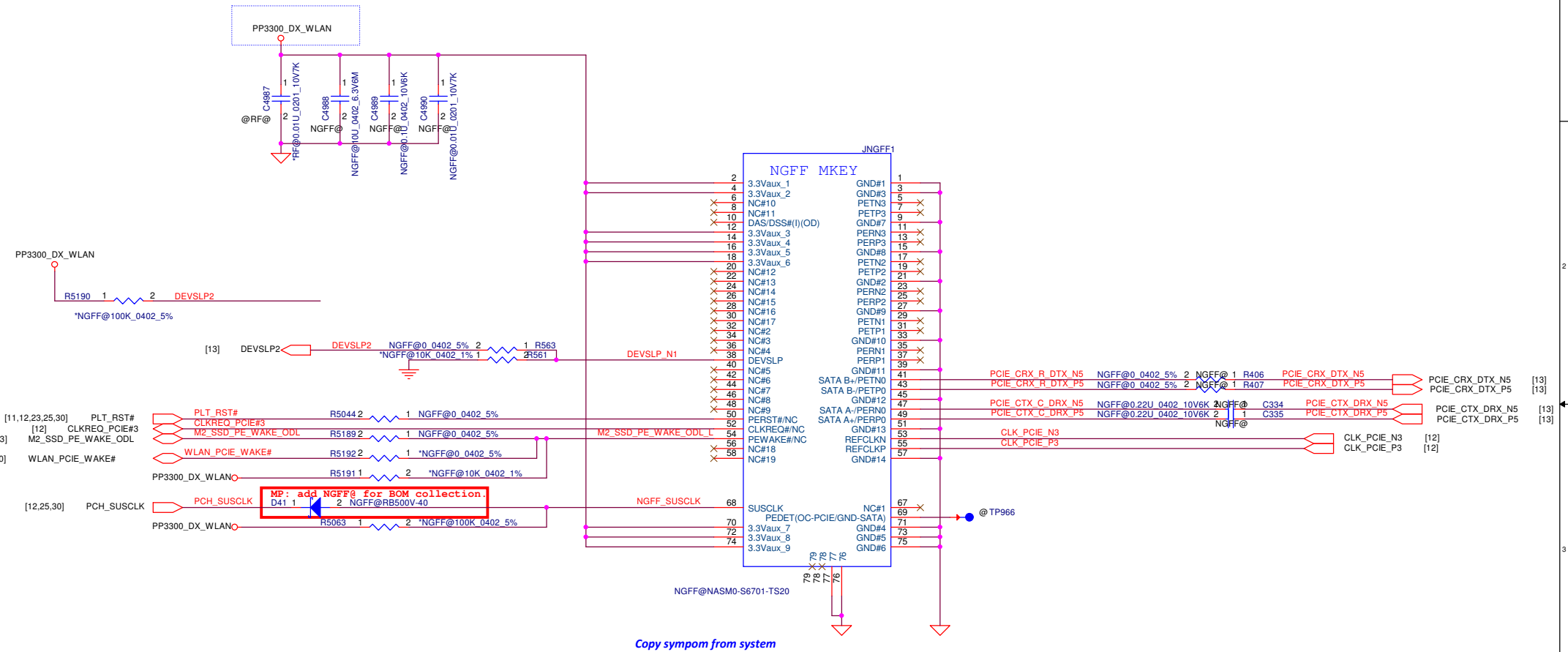
*JEDP1 change to DFFC40FR070, copy from ZSA*



## Touch Panel

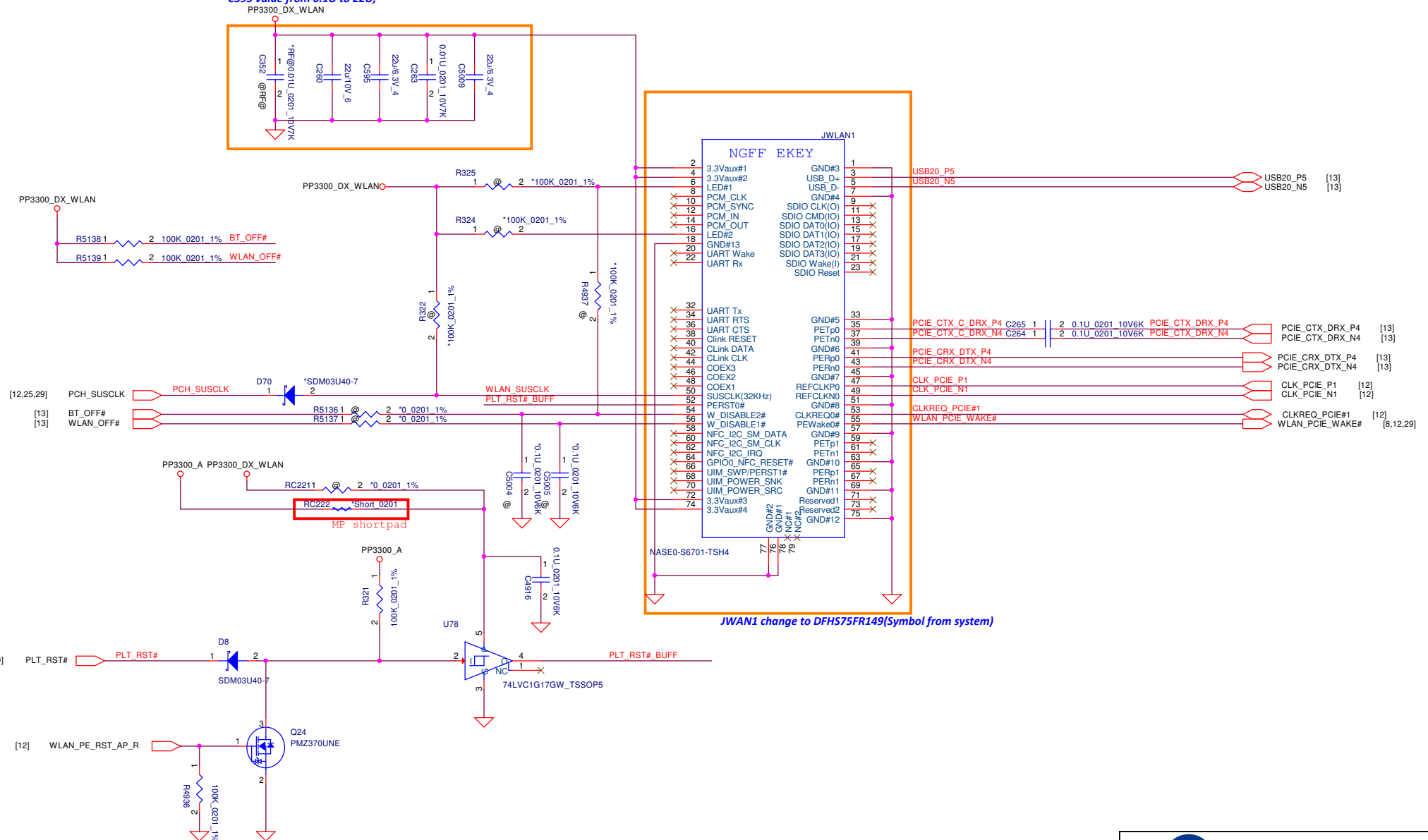


# KEY M

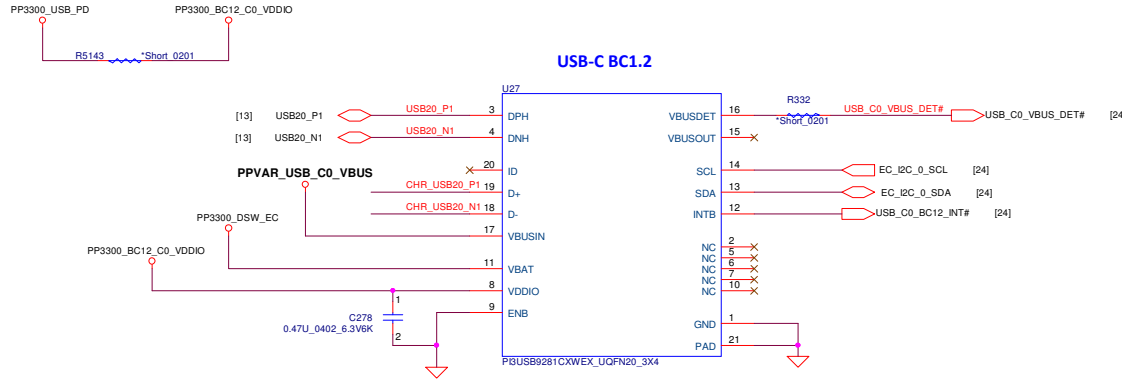
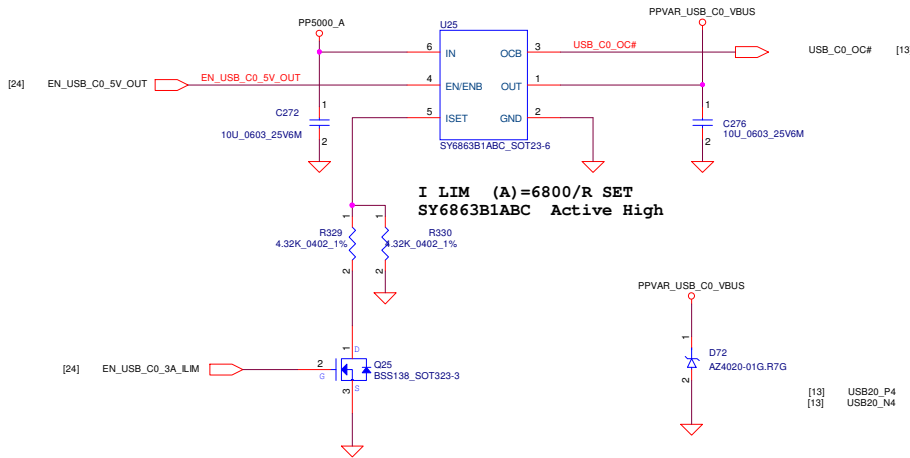


## NGFF WiFi/BT (KEY E)

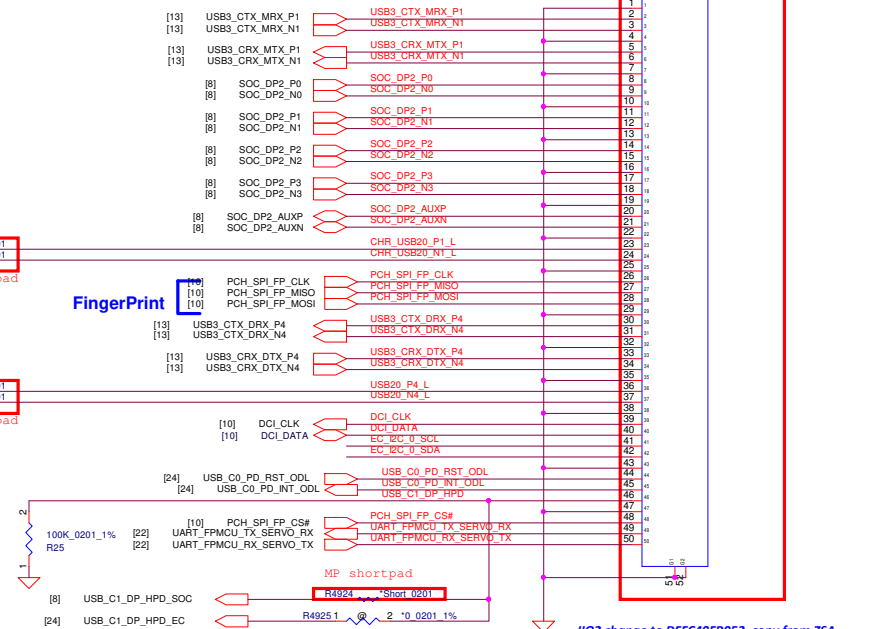
To meet Intel wifi spec: chagne C260 value from 10U to 22U,  
C595 value from 0.1U to 22U,



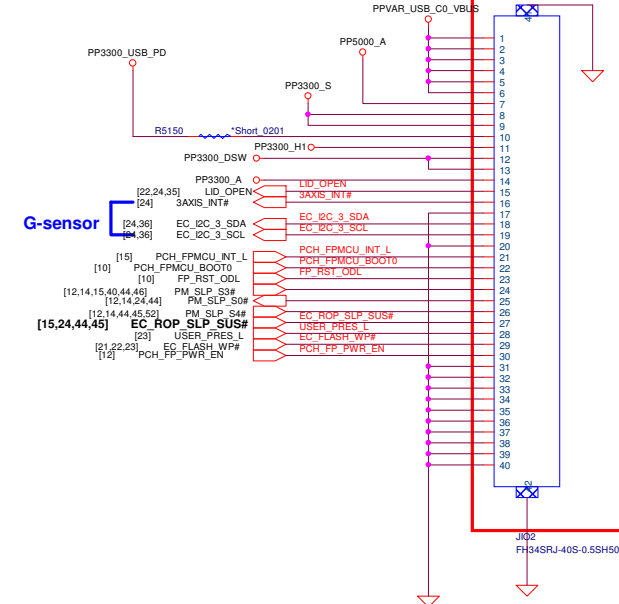
# TYPE-C 5V POWER SWITCH



## Fingerprint

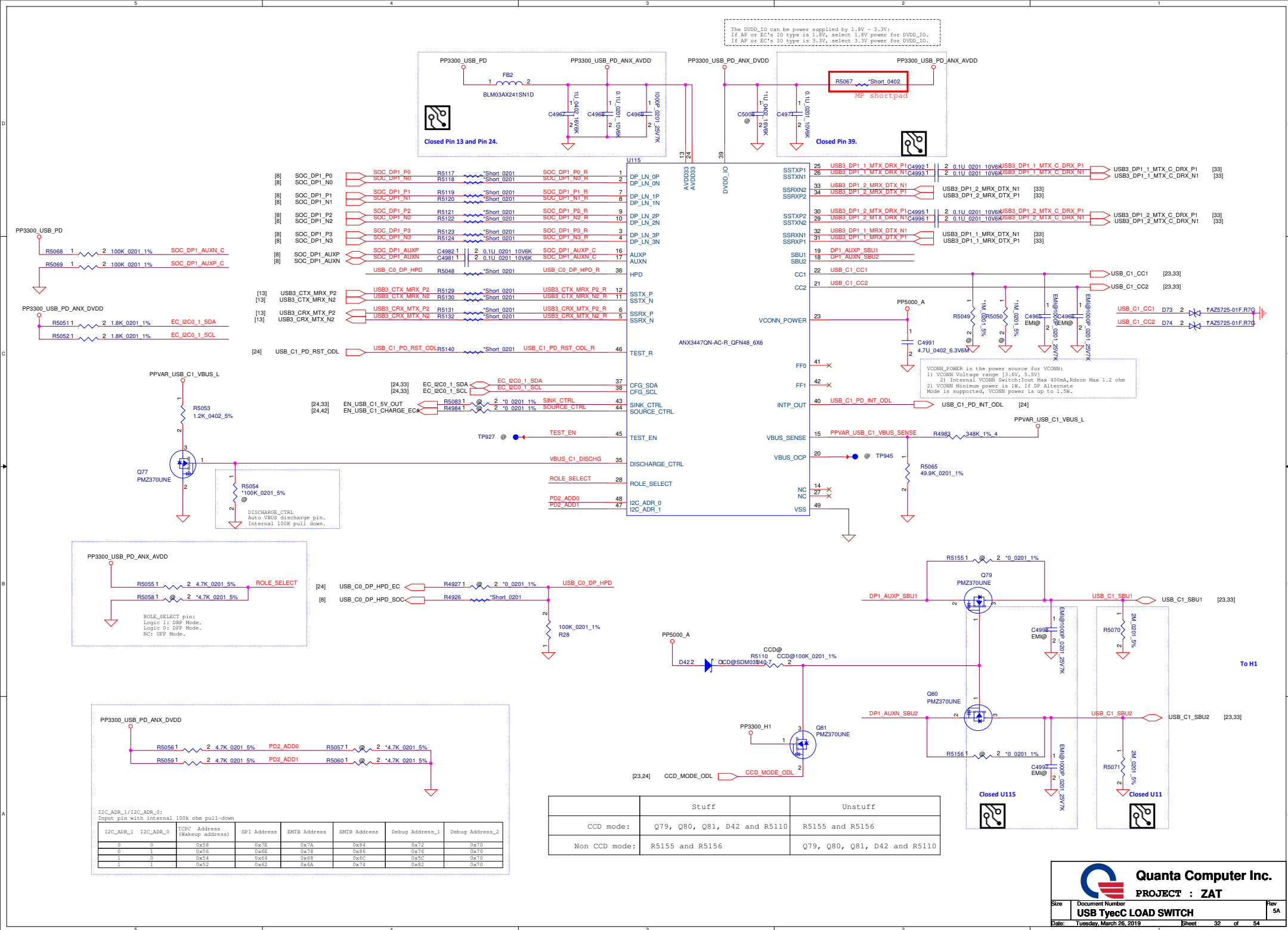


## G-sensor



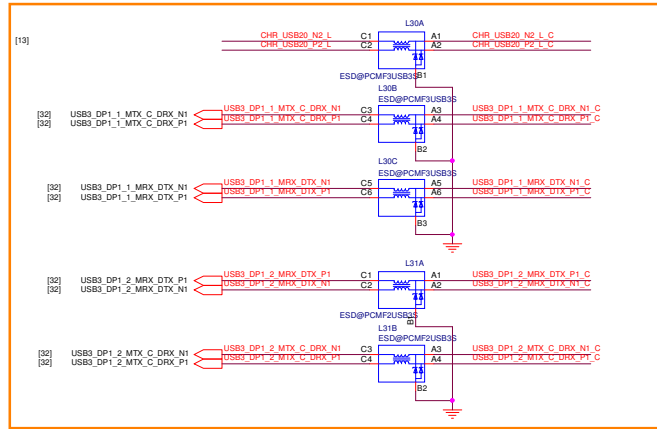
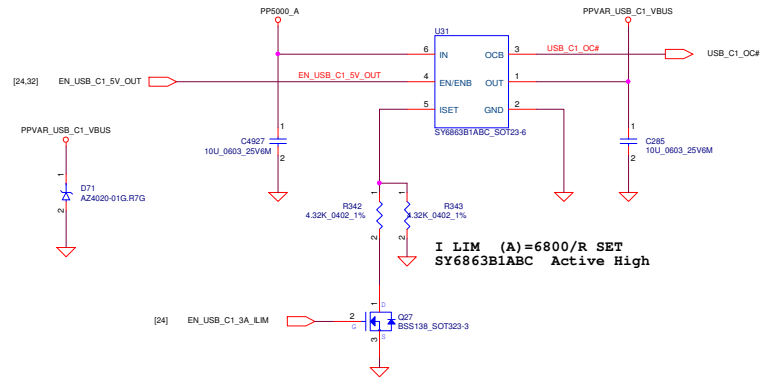
J101 change to DFFC50FR048,copy from 0CF  
 0325 MP change PCB footprint

J102 change to DFFC40FR052, copy from ZSA  
 0325 MP change PCB footprint

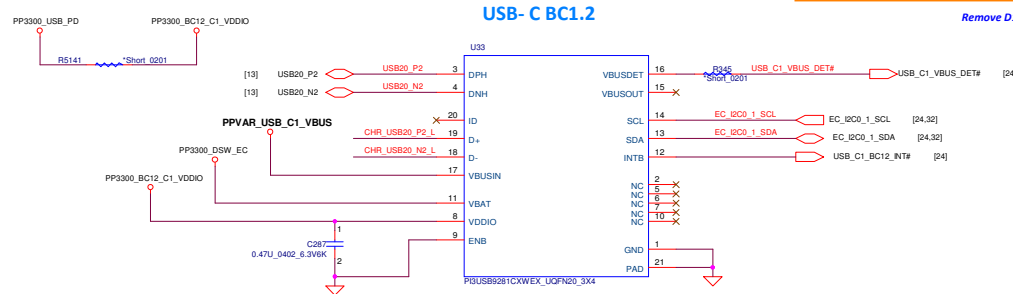




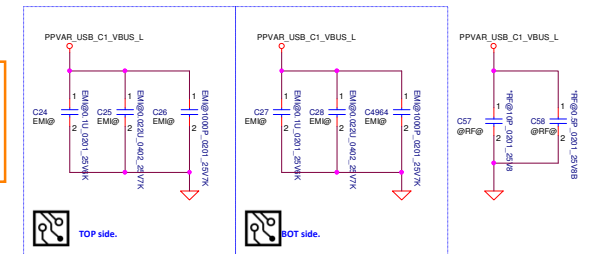
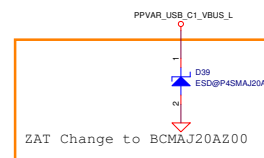
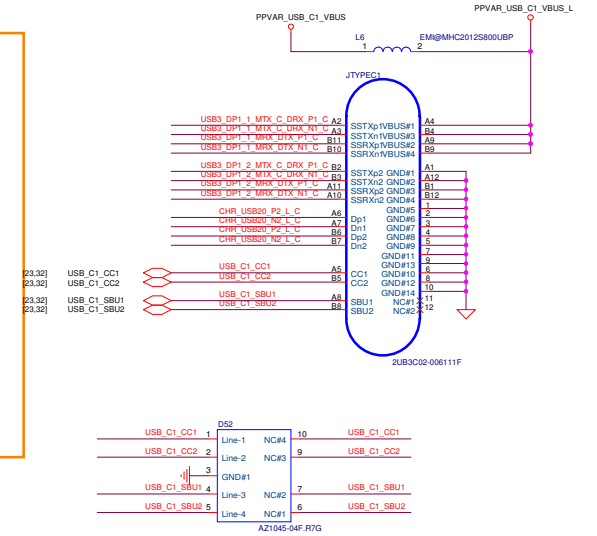
## 5V Current limit

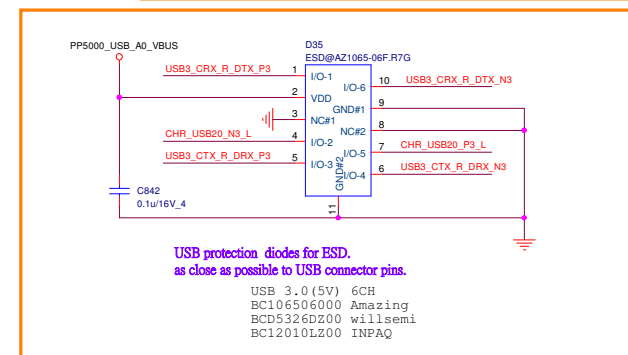
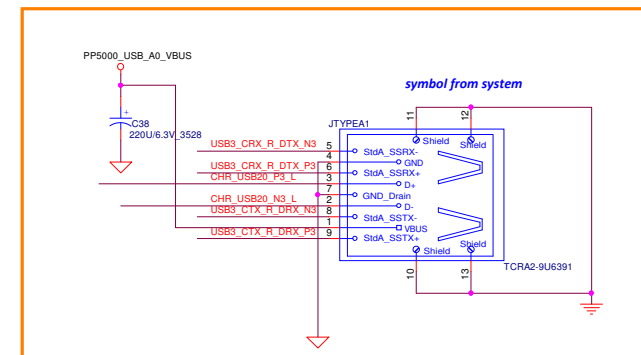
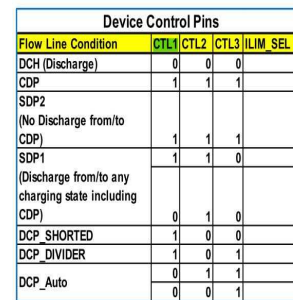



Remove D11/D12/D13/D27/D28/D29/D30/D31/D40 and change to L30/L31/D52

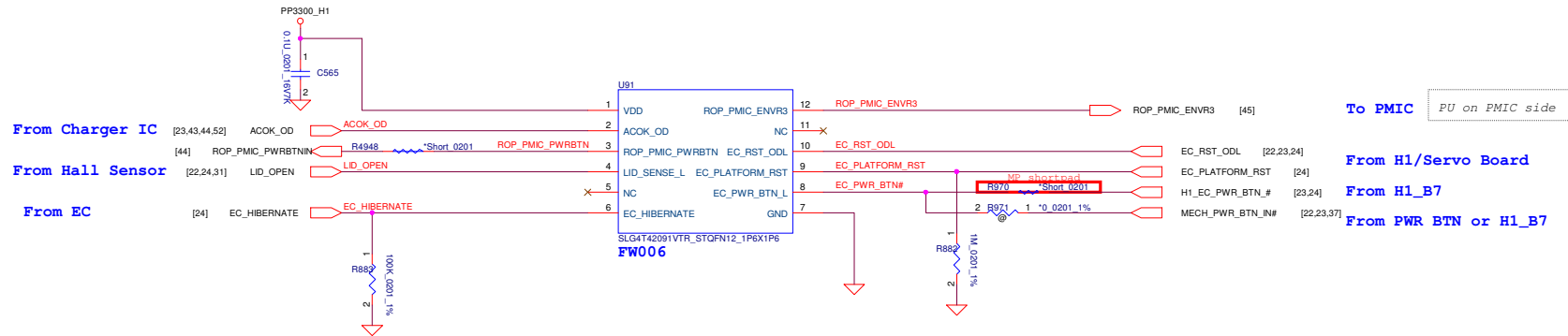


## USB TYPE-C Conn





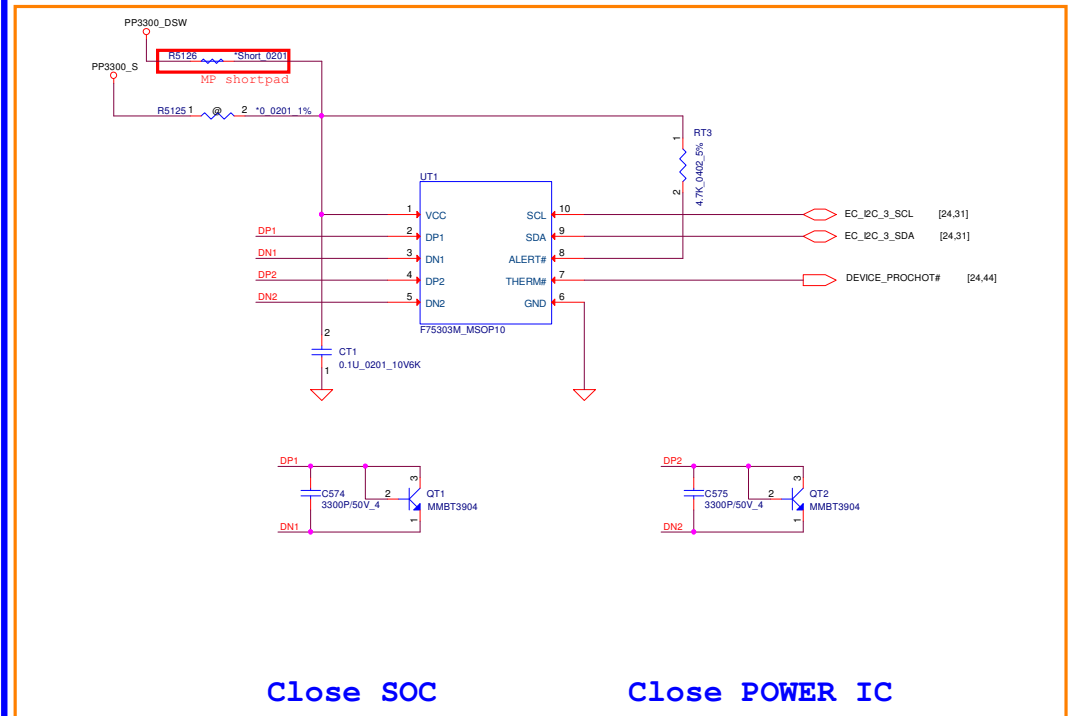
 <div> <b>Quanta Computer Inc.</b>  <b>PROJECT : ZAT</b> </div>		
Size	Document Number	Rev
	<b>USB Type-A / LED</b>	5A
Date:	Tuesday, March 26, 2019	Sheet 34 of 54



## Pin Configuration

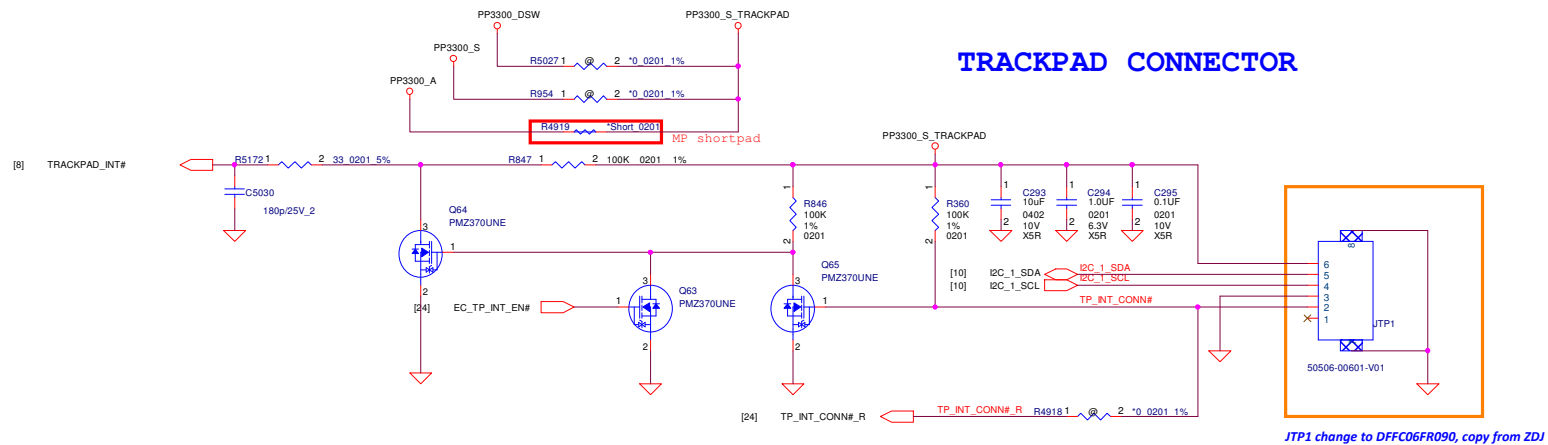
Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	ACOK_OD	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	ROP_PMIC_PWRBTN	Digital Output	Open Drain NMOS 1X	floating
4	LID_SENSE_L	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
5	NC	--	Keep Floating or Connect to GND	--
6	EC_HIBERNATE	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
7	GND	GND	Ground	--
8	EC_PWR_BTN_L	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
9	EC_PLATFORM_RST	Digital Input	Digital Input with Schmitt trigger	1MΩ pulldown
10	EC_RST_ODL	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	100kΩ pullup
11	NC	--	Keep Floating or Connect to GND	--
12	ROP_PMIC_ENVR3	Digital Output	Open Drain NMOS 1X	floating

## Thermal Sensor

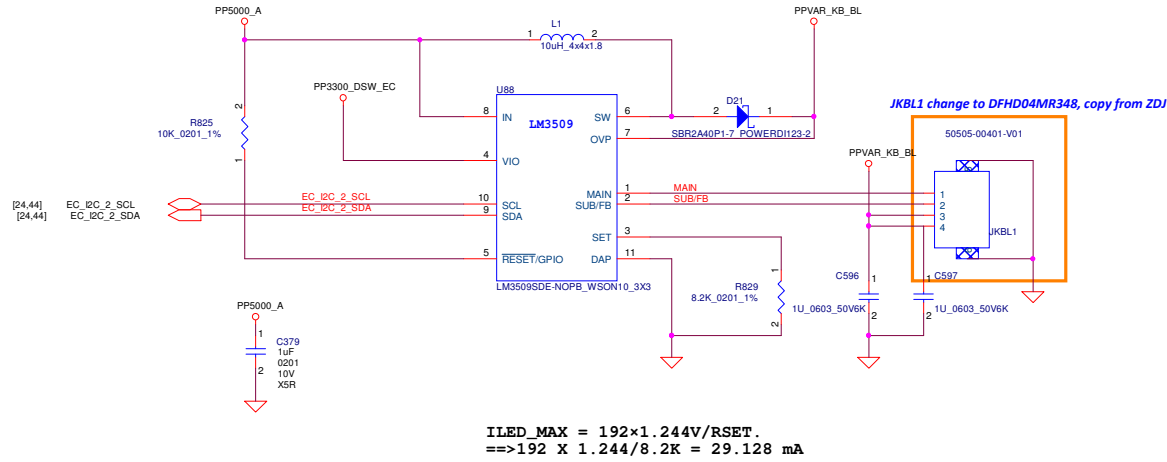


Change Thermal sense circuit and copy from ZAS

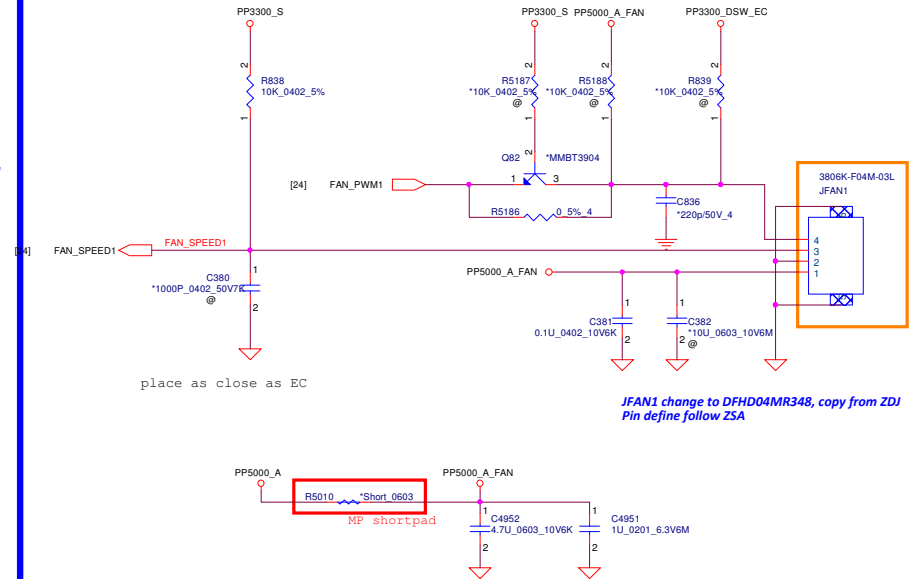
## TRACKPAD CONNECTOR



## KEYBOARD BACKLIGHT

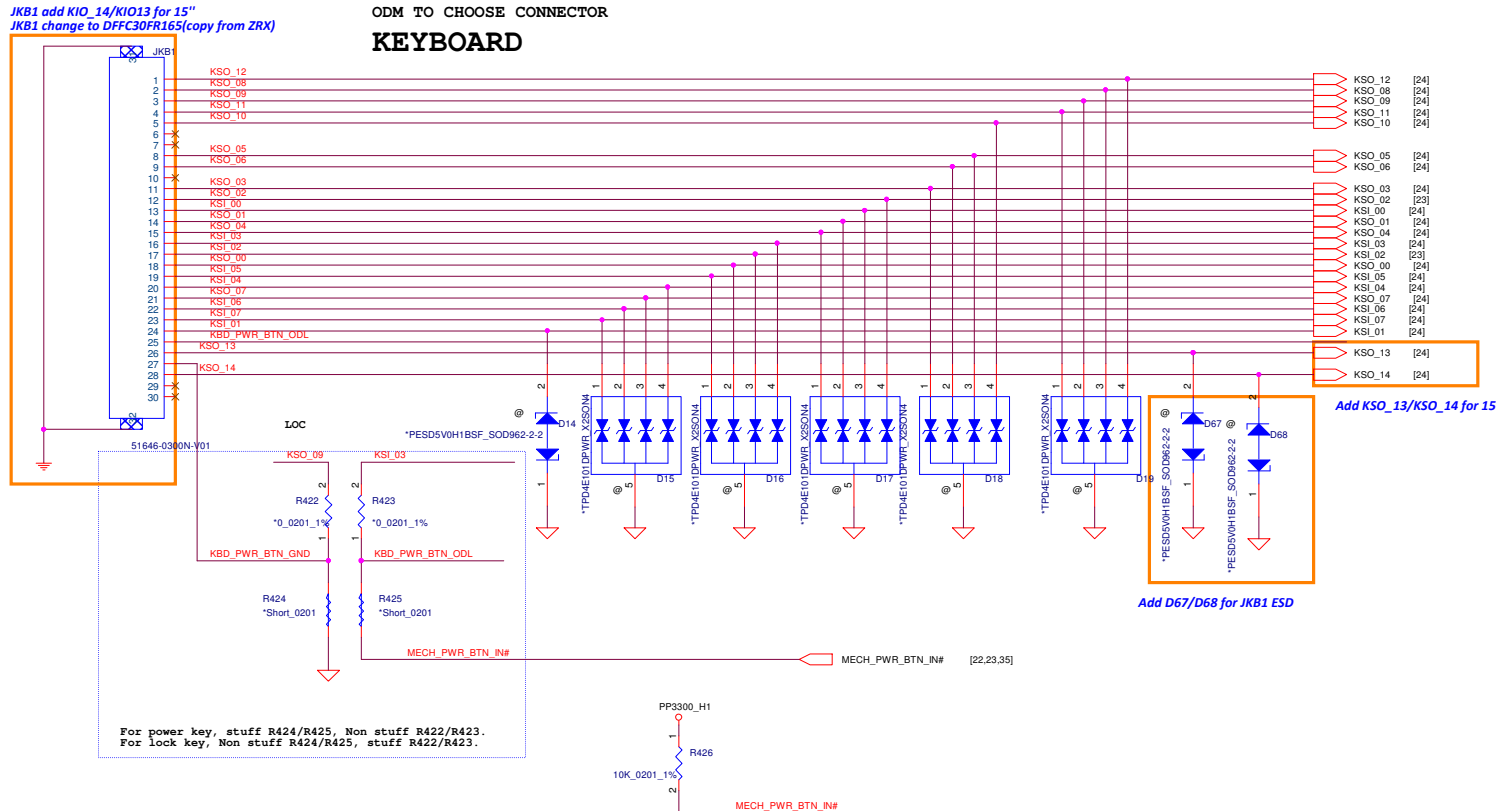


## CPU Fan Control Circuit



ODM TO CHOOSE CONNECTOR

## KEYBOARD



Quanta Computer Inc.

PROJECT : ZAT

	A	B	C	D	E
1					
2					
3					
4					

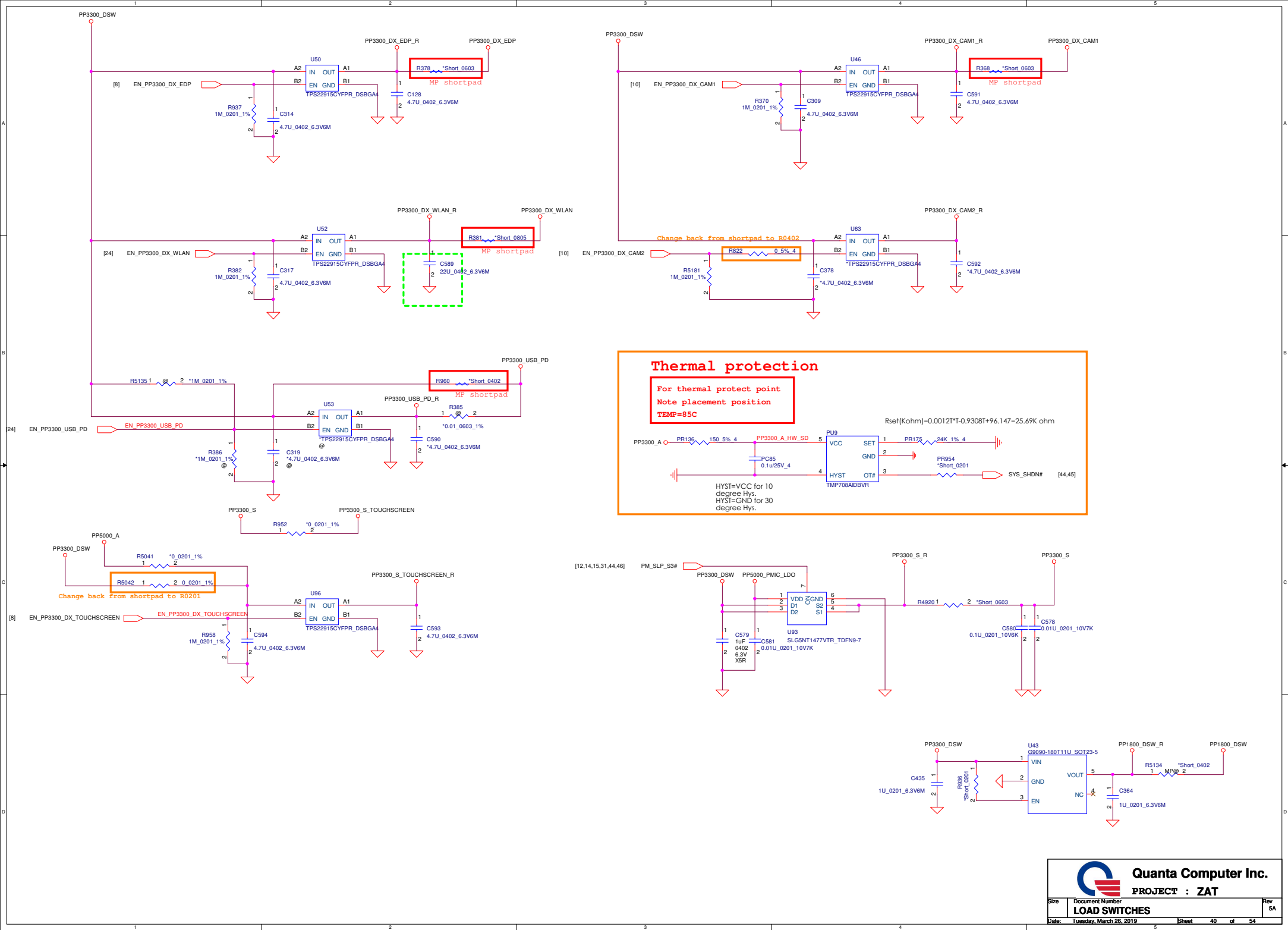


**Quanta Computer Inc.**  
**PROJECT : ZAT**

Size	Document Number	Rev
	<b>Finger Print</b>	5A
Date:	Tuesday, March 26, 2019	Sheet 38 of 54

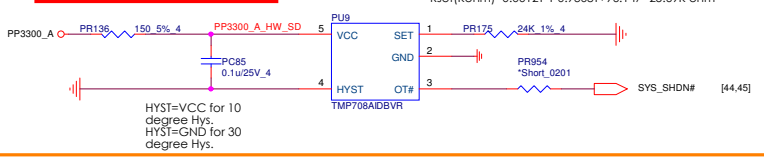






**Thermal protection**

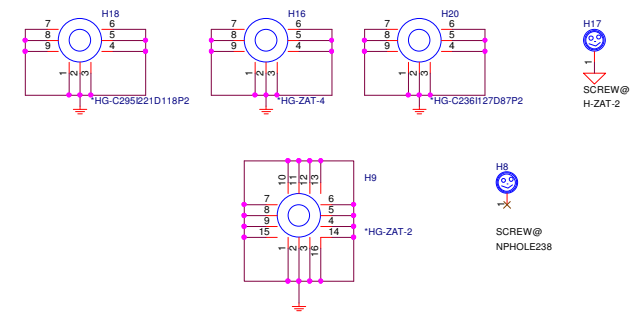
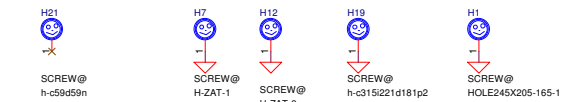
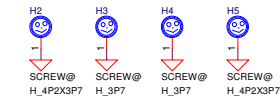
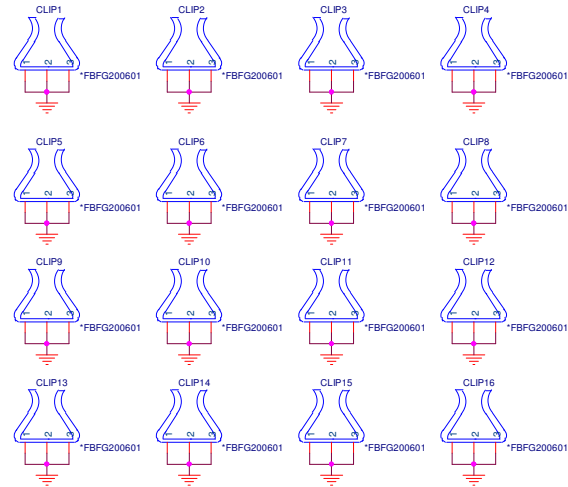
For thermal protect point  
Note placement position  
TEMP=85C

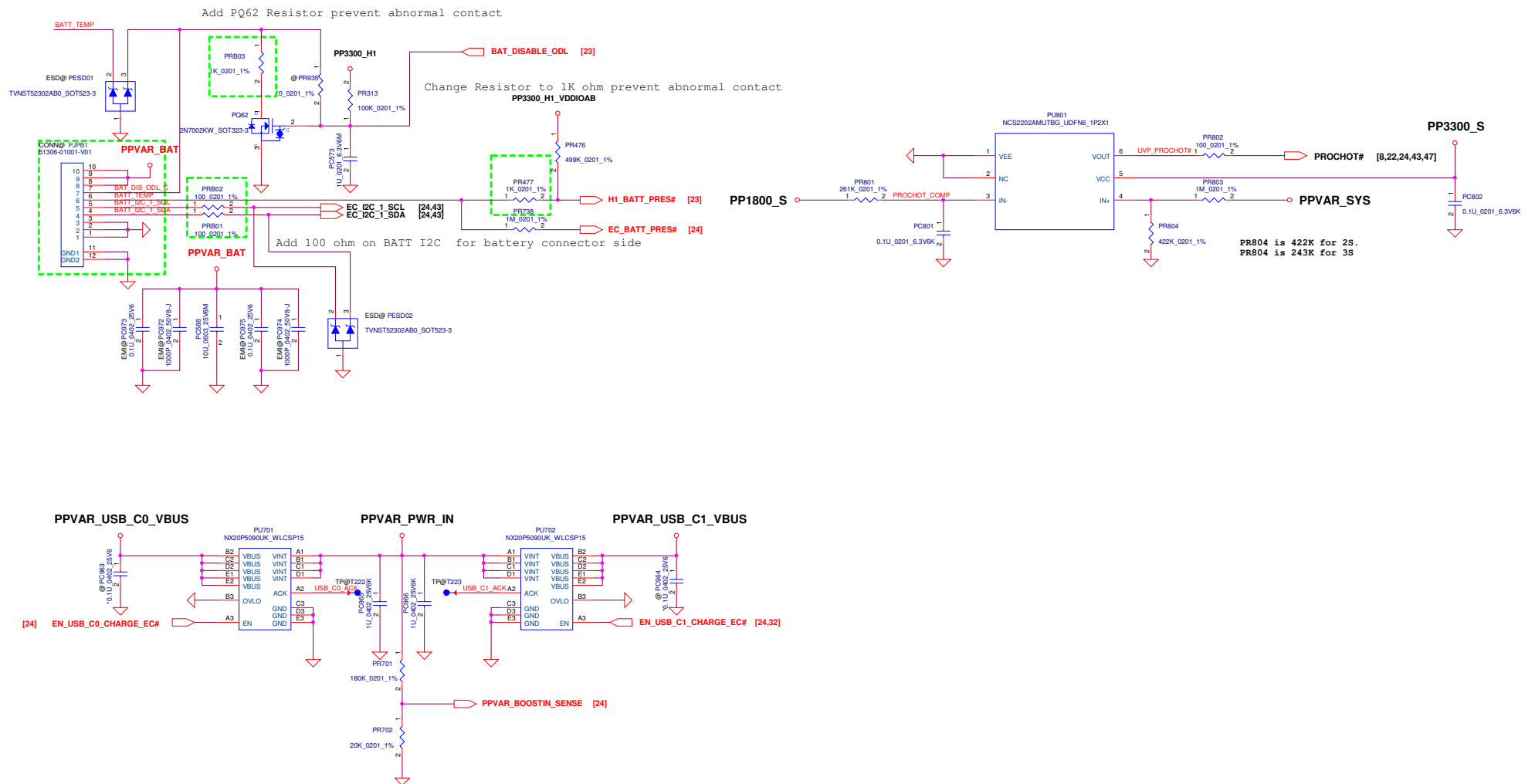


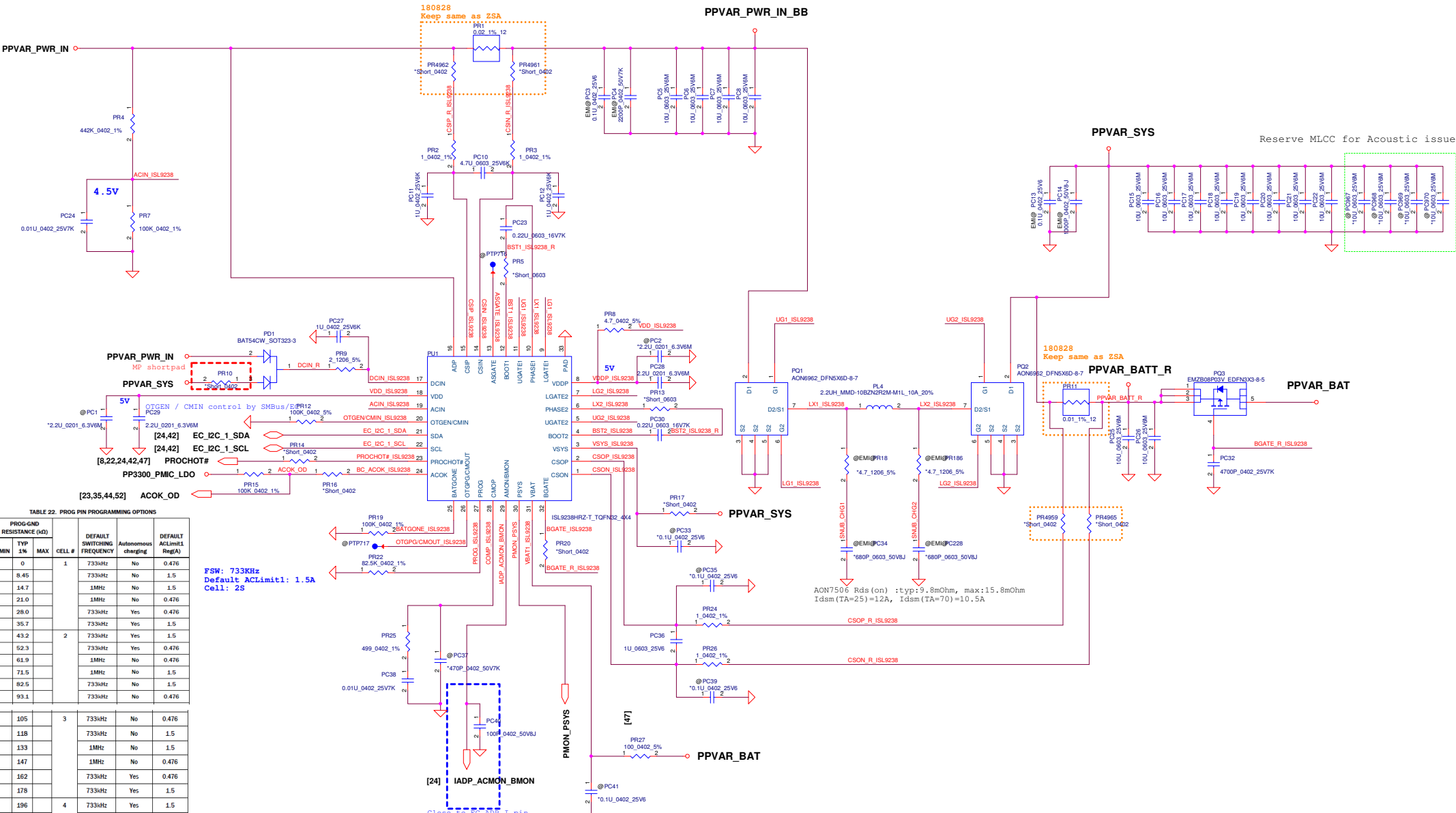
# [PCB]

# [CLIP]

# [Screw Hole]

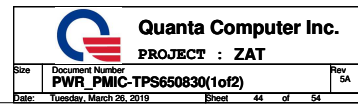


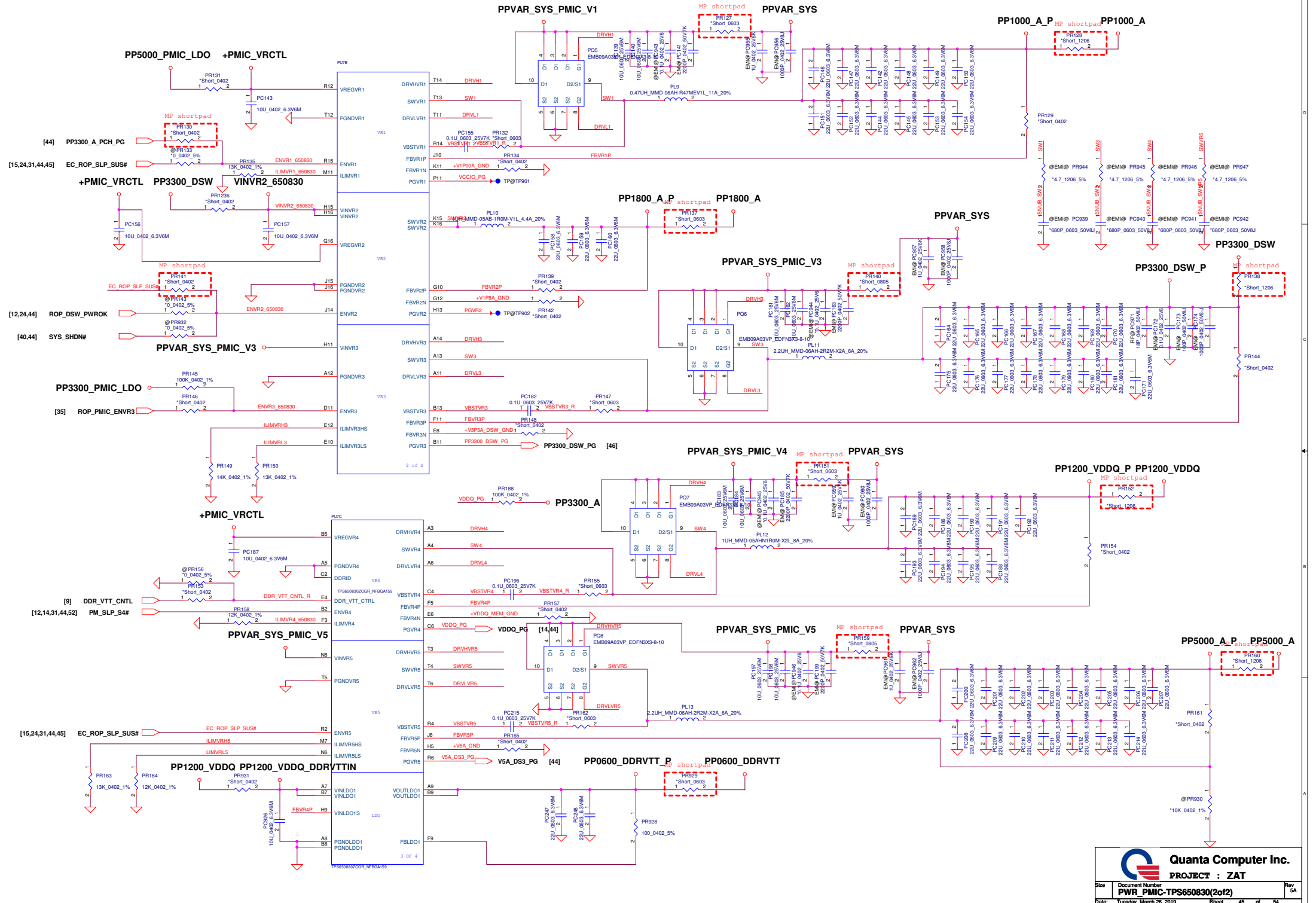


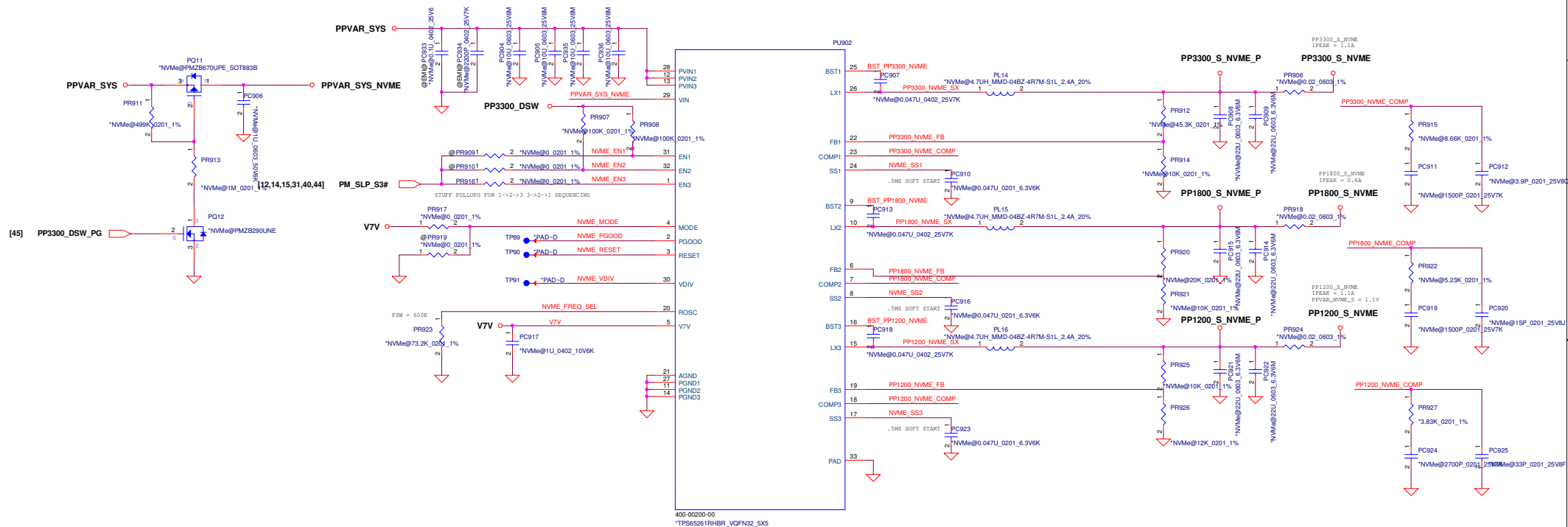


PROG-GND RESISTANCE (kΩ)		MIN	TYP 1	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIMIT1 REG(A)
					1	733kHz	No	0.476
8.45						733kHz	No	1.5
14.7						1MHz	No	1.5
21.0						1MHz	No	0.476
28.0						733kHz	Yes	0.476
35.7					2	733kHz	Yes	1.5
43.2						733kHz	Yes	1.5
52.3						733kHz	Yes	0.476
61.9						1MHz	No	0.476
71.5						1MHz	No	1.5
82.5					733kHz	No	1.5	
93.1					733kHz	No	0.476	

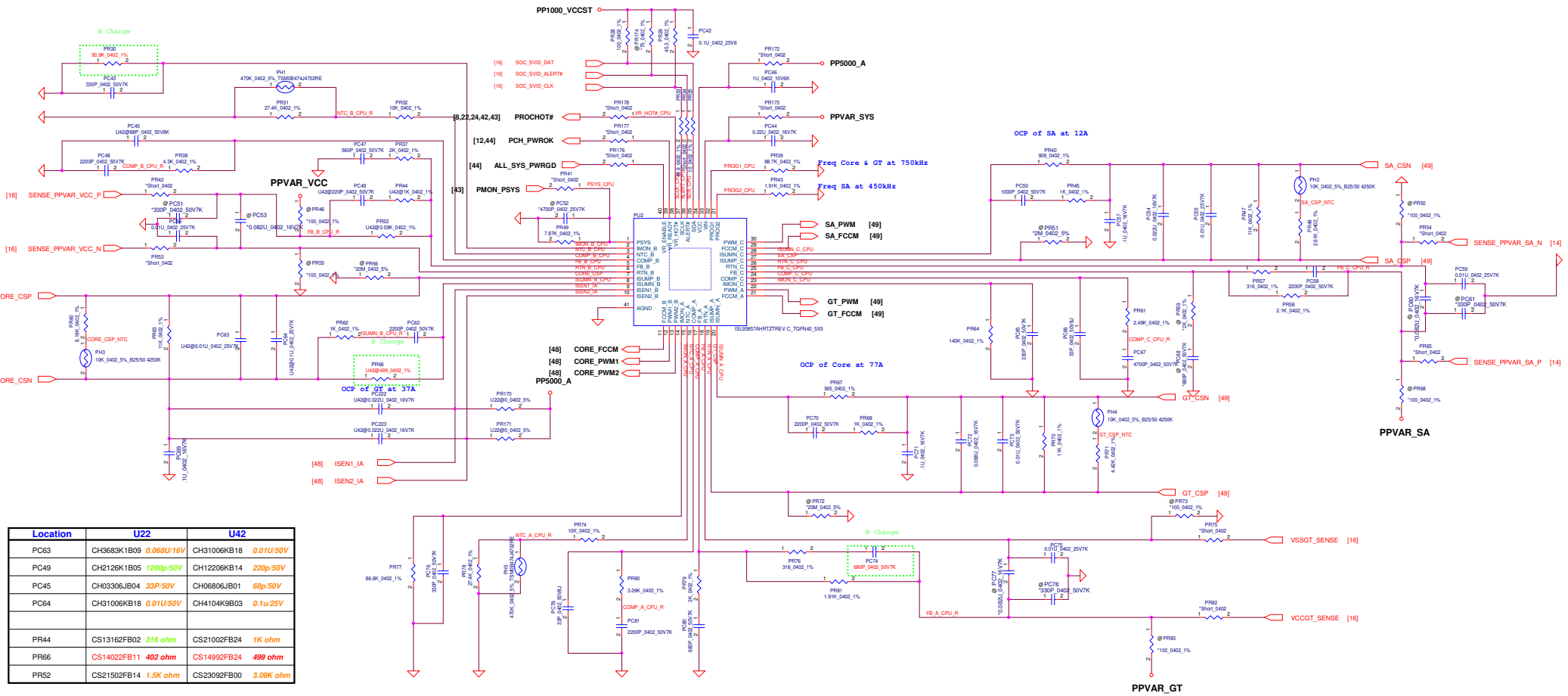
Fsw: 733KHz  
Default ACLimit1: 1.5A  
Cell: 2S











Location	U22	U42
PC63	CH3683K1B09 0.068U/16V	CH31006KB18 0.01U/50V
PC49	CH2126K1B05 1200p/50V	CH12206KB14 220p/50V
PC45	CH03306JB04 33p/50V	CH06806JB01 68p/50V
PC64	CH31006KB18 0.01U/50V	CH4104K9B03 0.1u/25V
PR44	CS13162FB02 316 ohm	CS21002FB24 1K ohm
PR66	CS14022FB11 402 ohm	CS14992FB24 499 ohm
PR52	CS21502FB14 1.5K ohm	CS23092FB00 3.09K ohm

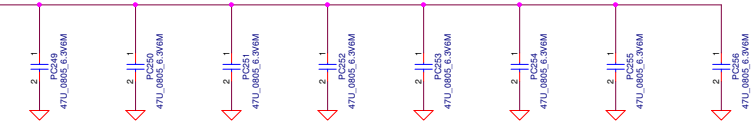
Location	U22	U42
PC222	N/A	CH32203KB11 0.022U/16V
PC223	N/A	CH32203KB11 0.022U/16V
PR170	CS00002JB38 0 ohm	N/A
PR171	CS00002JB38 0 ohm	N/A



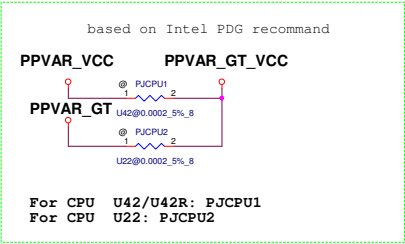
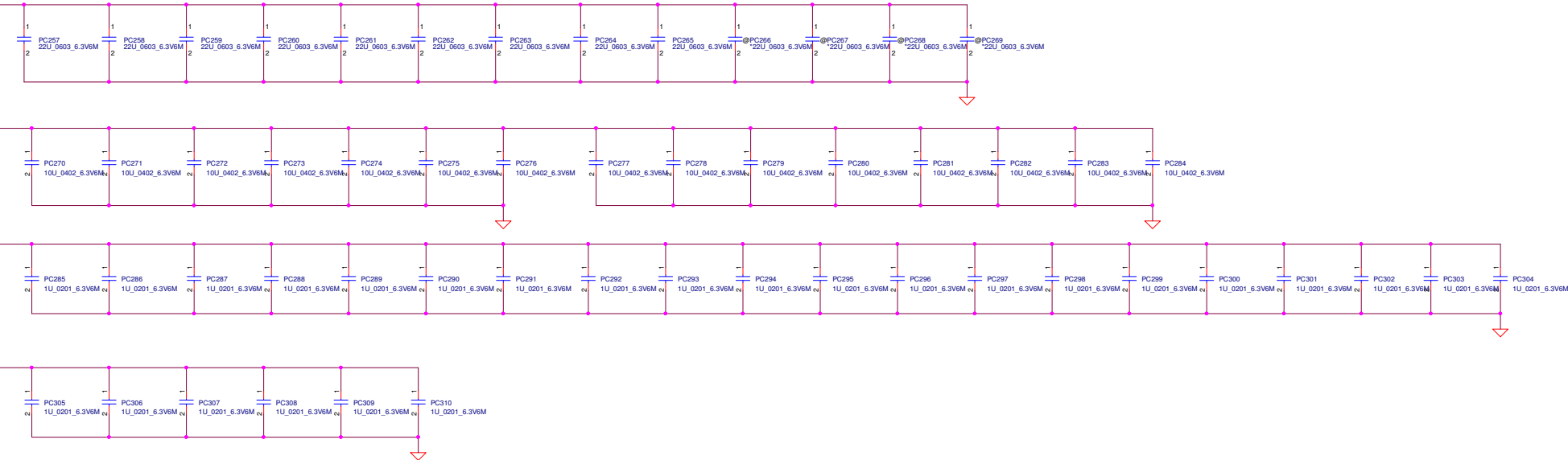


+VCC\_CORE  
220U\_R9 \* 3 pcs  
47U\_0805 \* 8 pcs  
22U\_0603 \* 9 pcs  
10U\_0402 \* 7 pcs  
1U\_0201 \* 26 pcs

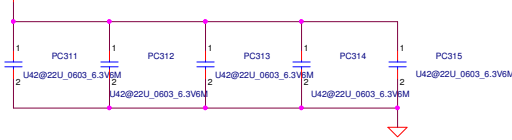
PPVAR\_VCC



CAPS PLACE ON OPPOSITE SIDE OF SOC

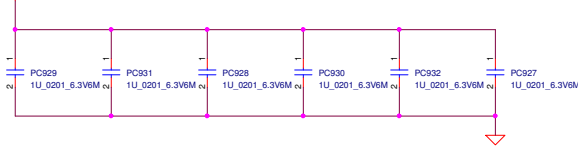


PPVAR\_VCC



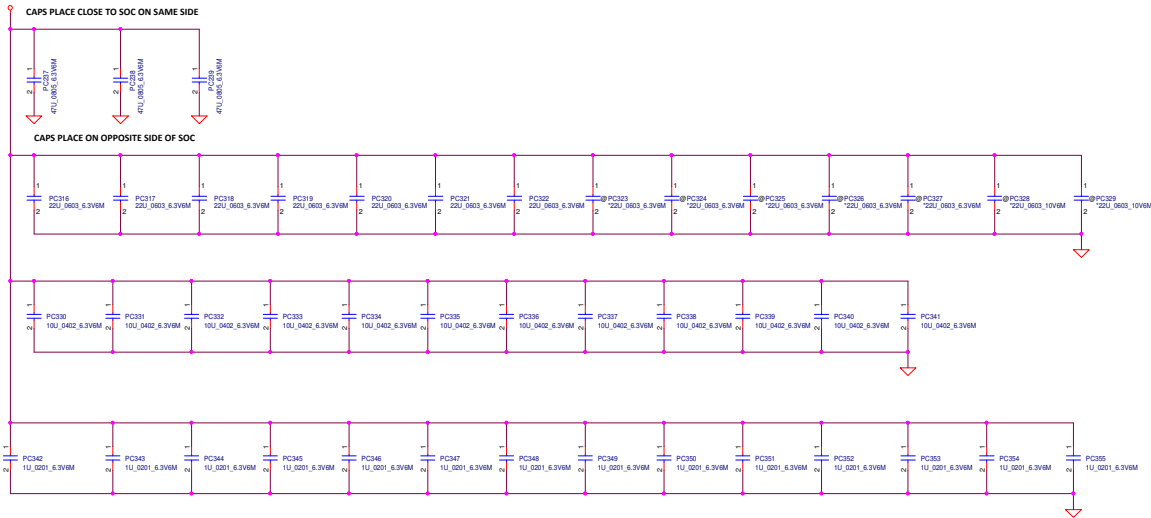
Based on Intel PDG recommand

PPVAR\_GT\_VCC



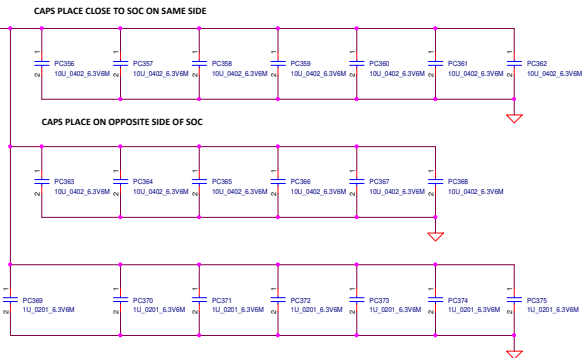
+VCC\_GT  
 220U\_R9 \* 2 pcs  
 47U\_0805 \* 3 pcs  
 22U\_0603 \* 7 pcs  
 10U\_0402 \* 12 pcs  
 1U\_0201 \* 14 pcs

# PPVAR\_GT

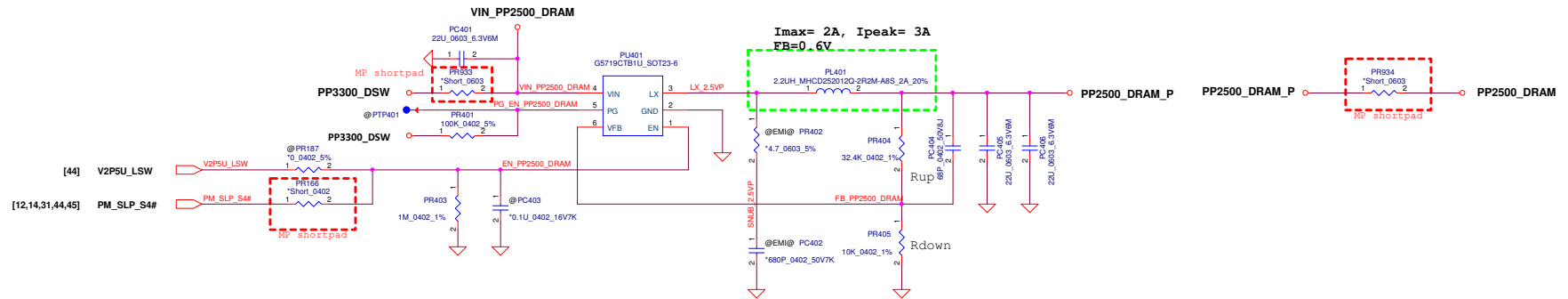


+VCC\_SA  
 10U\_0402 \* 13 pcs  
 1U\_0201 \* 7 pcs

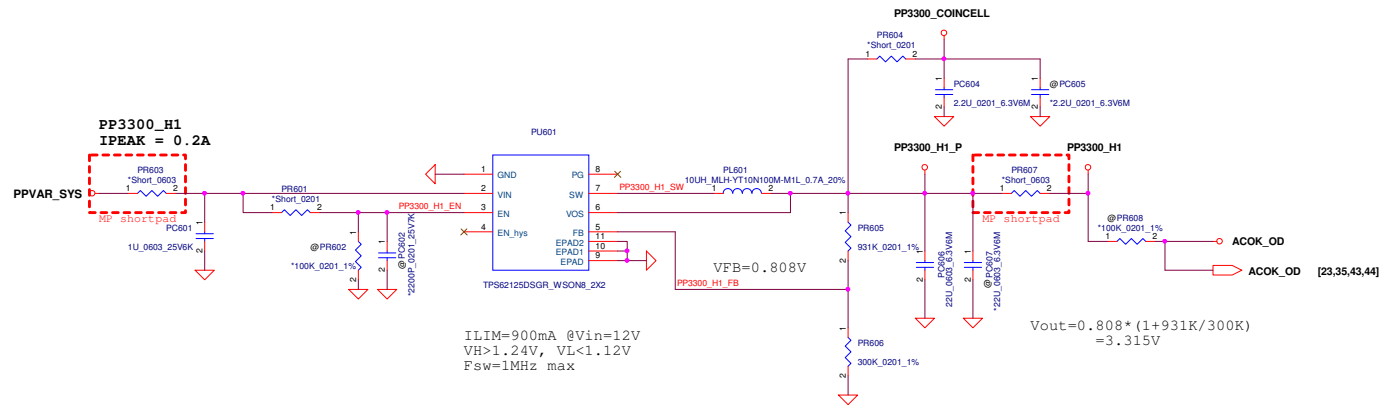
# PPVAR\_SA




# Change PP2500\_DRAM solution from G9661 to G5719 for Intel Deep S3 mode



Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage



Model		Version	CHANGE LIST		
		1A	<p>EE portion:</p> <p>P08:EDP_TX_N3EDP_TX_N2EDP_TX_P3EDP_TX_P2-&gt;remove (Nami is Rear Camera,ZAT don't need)</p> <p>P08:P31,SOC_DP2_CTR1,CLK and SOC_DP2_CTR1_DATA,Remove connection to J02</p> <p>P10:Remove UCI_M2,PEN_BQ0 and UCI_M3,PEN_PDCT4 out connection and UCI_L4,PEN_RST0 set TP963</p> <p>P10:Key R4905/R494 pull high with PP1000_S_PEN at P10</p> <p>P10:Remove IDC_2_SDA, PEN12C_2_SCL_PEN and R972/R973 and Set TP952/TP951,Unstuff R782/R792</p> <p>P10:Change PP_INT to PCH_FPMCUC_INT_I</p> <p>P10:Remove TP26-TP32 to connect with U116</p> <p>P10:UCIE1M4 to connect PCH_FPMCUC_ROOTWUCIEN3 connect to PCH_MPMCUC_INT_I</p> <p>P10:P31:Remove IDC_3_SDA,RVDC_3_SCL_R1 and R96/R96d from J02</p> <p>P10:P36:Remove TRACKPAD_DISABLE0 from JTP1 and set TP961</p> <p>P11:Remove L20/R4952/SOC_DMIC_CLK1_R/SOC_DMIC_DATA1_R/CSS5/C356</p> <p>P11:Remove C4920 and DS_1_MCLK_R1</p> <p>P10:P31:Remove DS_1_BCLK_RU2S_1_MCLK_RU2S_1_TX_R1,ADC12S_1_FS_R1,LRC_due to no related function</p> <p>P10:P36:Remove L20/R4952/SOC_DMIC_CLK1/SOC_DMIC_DATA1/C356/C357/U114/R501/C491/R508S/R508W/JCAM1/D26/L12/R5017/R5018"</p> <p>P12:Change C34WC340/C97CKC98 value from 50V to 25 V</p> <p>P12:U4 change to AL001G08050,copy from ZSA</p> <p>P12:P25:C7P/C78/C340/C34WC494/C4915 change to CH0154J003/Nami spec is 50,We only have 25V)</p> <p>P13:P22:P24/P30/P34P34P36/Q404/Q405/P730/TX24/Q754/Q757/Q760/Q770/Q790/Q800/Q1_COPY from ZSA</p> <p>P13:P29:Remove USB20_P40/USB20_N9 change to connect with TP956/TP957,remove from JNGFF1</p> <p>P13:P31:Key EMR_GARAGE_DET,GPP_EMER_GARAGE_DET,GPP_E1 and EMR_GARAGE_DET change to TP955,EMR_GARAGE_DET remove from J02</p> <p>P13:P31:USB20_N60/USB20_P6 change to connect with TP958/TP959</p> <p>P19:P30:RD12/RD61 change footprint from 0201 to 0402</p> <p>P21:U5 change to AKE37FN00N00 copy from ZSA</p> <p>P21:U7 change to AKE37FN00N4 copy from ZSA</p> <p>P22:Remove TP5757 to add UART_FPMCUC_RX_SERVO_TX,UART_FPMCUC_TX_SERVO_RX</p> <p>P22:Add RS168-RS171 for UART_FPMCUC_RX_SERVO_TX/H1_BOOT_UART_RX/H1_BOOT_UART_TX,UART_FPMCUC_TX_SERVO_RX</p> <p>P24:U10 change to AKE3AZBK603</p> <p>P24:Remove R4912/R4914</p> <p>P24:Change U103 to AKE3AZBK603,copy from ZSA</p> <p>P24:RSU11 unstuff for read IC_FV006</p> <p>P24:P31:Remove EC_CHG_LED_W_R1/EC_CHG_LED_Y_R1/R965/R967</p> <p>P24:P31:Remove EC_VOLDIN,BTENC_VOLDIN_BT from J02</p> <p>P24:P31:Remove TABLET_MODE from J02</p> <p>P24:P31:Remove 6AXIS_INTN from J02 and set TP960</p> <p>P24:P31:Remove AL3_INTN from J02 and set TP962</p> <p>P29:P32:1D2/D4/D2 change to B C08U340Z02 follow ZSA</p> <p>P26:HP1 change to DFT100/R973 copy from ZSA</p> <p>P26:D6/D7/D32 change to BCD111HSZ00 and add D64/D59/D61</p> <p>P27:D10 change to B C08532Z00 and add D66</p> <p>P27:D33 change to B C08532Z00 and add D65</p> <p>P27:INPK1 copy from ZSA/Some P/N J-P change to with-S0278-00401-v01-4p4</p> <p>P28:D34 change to B C08532Z00 and add D62</p> <p>P28:Add R394/R5086 for MIC power rail</p> <p>P28:Set PP1800_S_MIC to be Mic power and power source for PP1800_A</p> <p>P28:Remove PP3300_S_PEN with C372/C371/R395/R5085</p> <p>P28:Remove PP1800_S_PEN with C32/C34/R5086/R394/R4905/R4904</p> <p>P28:Remove U36/R400/R3905/R397/JE1R1</p> <p>P28:Remove TP5000_A_TOUCHSCREEN with C291/C292 and remove from J02</p> <p>P28:Remove C231-C234,C2EDP_TX_P2,C2EDP_TX_N2,C2EDP_TX_P3,C2EDP_TX_N3,C from JEDP1</p> <p>P28:JEDP1 change to DFFC40FR070,copy from ZSA</p> <p>P28:Idt PP3300_DSX_SENSE0R from J02</p> <p>P28:Add C5012 on PP3300_DSX_EDP</p> <p>P29:Copy symbol from system and change PN to DFHS75R371</p> <p>P29:Remove WLAN_PCIE_WAKE/OUT_OF_WLAN_OUT/PCU_SUSCLK/CLKREQ_PCIE03/WLAN_PCIE_WAKE#</p> <p>P29:Remove TP937-TP944</p> <p>P30:To meet limit with spec:change C360 value from 10U to 22U,C395 value from 0.1U to 22U, del C5011/C5010</p> <p>P30:JWANI change to DFHS75R140(Symbol from system)</p> <p>P30:To meet limit with spec:change C360 value from 10U to 22U,C395 value from 0.1U to 22U, del C5011/C5010</p> <p>P31:J01 change to DFFC50FR088,copy from ICF</p> <p>P31:J02 change to DFFC40FR082,copy from ZSA</p> <p>P31:Remove HP_IRQ_GPO from J02</p> <p>P31:MECH_PWR_BTN_IN0 from J02</p> <p>P33:TTY_PEC1 change to DFHS24R413 (Symbol and copy from ZAK)</p> <p>P33:Remove D11/D12/D13/D2/D28/D29/D30/D31/D40 and change to L30131/D52</p> <p>P33:D39 change to B C182LPS200</p> <p>P34:Remove D35/D38 change to D35/B C10656000</p> <p>P34:TTY_PEA1</p> <p>P34:ED1 follow ZSA,BE1000G2A0</p> <p>P34:C38 change to CH721M6600</p> <p>P34:TTY_PEA1 symbol use DFHS09FR706(Confirm with RDC),new F/P is ub3-6cr2-9v1901-9p</p> <p>P36:JTP1 change to DFFC30FR090,copy from ZJD</p> <p>P37:JFAN1 change to DFHD04MR348,copy from ZJD,Pin define follow ZSA</p> <p>P37:JKB1/JFAN1 change to DFHD04MR348,copy from ZJD</p> <p>P37:Add D67/D68 for JKB1 ESD</p> <p>P37:Add K50_13V50_14 for I57</p> <p>P37:JKB1 change to DFFC30FR165(copy from ZRX)</p> <p>P37:R426 put MECH_PWR_BTN_IN0 to connect with PP3300_I1 for pull high to P37</p> <p>P37:For power key, stuff R424/R425, Non stuff R422/R423</p> <p>P38:Add U116 Finger print function</p> <p>P38:Remove U107/U116 HALL IC to Sub-board</p> <p>P41:Add H17-H20</p> <p>P41:Change H17-H20 and HS value from layout request</p> <p>P105:Change R4905 power source from PP1800_S_PEN to PP1800_A</p> <p>P24:Remove TP962 and R4957</p> <p>P22:Follow Google guide to un-stuff RS158/RS171 for UART_FPMCUC_TX(RX)_SERVO</p> <p>P33:D39 change ESD solution to P45MAJ20A</p> <p>P10:P22/P25/P30/P32:Change D2/D4/D8/D9/D24 P/N to B C08U340Z02 follow ZSA</p> <p>P36:Add ESD solution,RS172,C5030 on TRACPAD_INTF</p> <p>P28:Add ESD solution,RS173,C5031 on EDP_HPD</p> <p>P24:R271 change value to 2.2kOhm and add C5032</p> <p>P8:Add ESD solution C1123 on PROCHOT#</p> <p>P13:Add ESD solution C5033 on USB_OC#</p> <p>P15:Add ESD solution C5034 on PP1000_PTL_A</p> <p>P15:Add ESD solution C5035 on PP1000_A</p> <p>P10:Remove PP circuit to Sub-board</p> <p>P29:Change Key E description Key M</p> <p>Power portion:</p> <p>P40 :Change C589 to 22uF</p> <p>P40 :Add P9,PR136,PC85,PR175,PR954 for acer HW shutdown sensor request (backup package test protection)</p> <p>P42 :Change P3PB1 Battery connector ace-S048S8-01001-v02 for acer new Battery pack and pin define revised.</p>		
		2A	<p>EE portion:</p> <p>P31:Change R329/R330/R342/R343 Footprint from 0201 to 0402 and P/N change from CS24321FE01 to CS24322FB14</p> <p>P12:CUVC4 change to 64pF to follow vendor suggestion</p>		
		3A	<p>EE portion:</p> <p>P10:Idt PCH_FPMCUC_INT_I from GPP_C8 &amp; GPP_P6 and change to test point about UCLAB1(TP946)/UCLN3 (TP965)</p> <p>P10:PCH_FPMCUC_INT_I add RS185 pull high with PP3300_A</p> <p>P15:UCLAN1/UCLAN3 add RS183/RS184 to connect with PCH_FPMCUC_INT_I</p>		
		4A	<p>EE portion:</p> <p>P37:add level shift circuit about Q82,RS186,RS187,C336 and RS188 into FAN_JFAN1/Mount R839 on JFAN1</p> <p>P8:P16,P12,P21,P23,P42,P25,P36,P28,P31,P32,P33,P35,P37:Change to D001 shortpad</p> <p>R6,R33,R56,R105,R124,R125,R136,R137,R138,R176,R177,R182,R188,R190,R194,R195,</p> <p>R196,R197,R198,R200,R206,R213,R14,R301,R332,R345,R424,R425,R879,R935,R948</p> <p>R849,R853,R854,R855,R856,R860,R862,R866,R904,R934,R961,R962,R966,R968,R4910,</p> <p>R4916,R4917,R4926,R4948,R506,R505,R506,R506,R5095,RS117,RS118,RS119,</p> <p>RS120,RS121,RS122,RS123,RS124,RS129,RS130,RS131,</p> <p>RS132,RS140,RS141,RS143,RS150,RS154</p> <p>P12,P16,P26,P40:Change to 0402 shortpad RC110,R822,R5004,RS178,RS183,RS184</p>		
DOC NO.	PROJECT MODEL	Chrome	APPROVED BY:	DATE:	
	PART NUMBER:		DRAWING BY:	REVISION:	
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